Broadband Micro-Coaxial Wilkinson Dividers

Negar Ehsan[(1)], Kenneth Vanhille[(1)], Sébastien Rondineau[(2)], Evan Cullens[(1)], Zoya Popović[(1)]

(1) Active Antenna Laboratory
University of Colorado at Boulder
USA

(2) Solentech – Solution, Engineering & Technology
Porto Alegre, RS – Brazil
s.rondineau@solentech.com.br

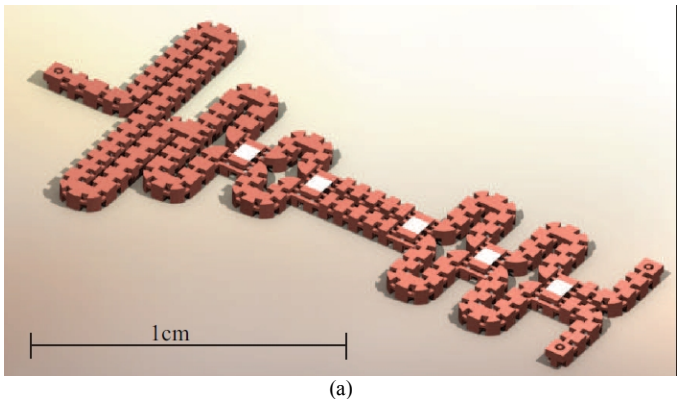
Abstract—**This paper presents several micro-coaxial broadband 2:1 Wilkinson power dividers operating from 2 to 22 GHz, a 11:1 bandwidth. Circuits are fabricated on silicon with PolyStrataTM technology, and are implemented with 650 um x 400 um air-supported micro-coaxial lines. The measured isolation between the output ports is greater than 11 dB and the return loss at each port is more than 13 dB over the entire bandwidth. The footprints of these dividers can be miniaturized due to the high isolation between adjacent coaxial lines and their tight bend radius. For higher power handling, larger lines with a cross-section of 1050 um x 850 um are also demonstrated. The effect of mismatch at the output ports is investigated, in order to find the power loss in the resistors.**

Keywords; Power dividers, coaxial components, coaxial transmission lines..

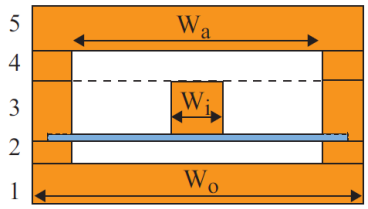
I. Introduction

The Wilkinson power divider was first introduced in 1960 as a distributed *N*-way circuit with *N*-1 lumped resistors [1]. Various distributed and lumped extensions of this in-phase high-isolation divider have been researched to date [2]. For a single-section two-way divider the bandwidth is around 3:1 for a VSWR of 2:1. Several methods have been developed to increase the bandwidth of such dividers. In 1968, Cohn introduced a multi-section divider, containing *M* pairs of equal-length transmission lines in series and *M* shunt resistors between the pairs [3]. This divider can theoretically achieve 10:1 bandwidth with *M* = 7, with an impedance range of 90 Ω–50 Ω and resistor values of 100 Ω–600 Ω. High isolation can be maintained between output ports over a broad bandwidth. Other broadband Wilkinson-type dividers are designed mostly in microstrip [4]. Algorithms to find the correct number of sections, characteristic impedances and lumped resistor values are given for ideal components [5], [6]. The greatest experimentally demonstrated bandwidth with the Wilkinson divider to the best of the authors' knowledge is 4:1 (3–12 GHz) using a stripline configuration with four sections [5].

The goal of this paper is to demonstrate broadband Wilkinson dividers implemented in wafer-scale PolyStrata™ technology [7], which provides both low loss and small footprints simultaneously; the latter is illustrated in Fig. 1 (a). The micro-coaxial lines are air-filled and fabricated using sequential metal deposition and standard photolithography. A large number of millimeter-wave narrowband components such as resonators, hybrids, and antennae have already been demonstrated with this process [8]–[10].



(a)



(b)

Fig. 1. (a) Rendering of the miniaturized 2–22 GHz Wilkinson divider implemented in the five-layer fabrication process. (b) Cross-section of the five-layer micro-coaxial line. The height of layers 1, 3, and 5 is 100 um, and layers 2 and 4 are 50 um tall. The inner conductor is supported by 100 um wide, 18 um tall dielectric straps that are embedded in the bottom of layer 3. W_o = 650 um, W_a = 450 um and W_i = 82:1 um are the dimensions for a 50 Ω line.

The PolyStrataTM micro-coaxial lines have loss as low as 0:1 dB/cm (0:08 dB/wavelength) at 38 GHz [11], and very high isolation of -60 dB at Ka band for neighboring lines sharing a common ground wall [12]. The characteristic impedance of the lines is constant over a broad range of frequencies, since the TEM mode is dominant up to around 450 GHz, depending on the line geometry [13]. The low dispersion, accompanied by low loss and high isolation, makes the PolyStrata™ process uniquely suitable for ultra-broadband miniaturized components, such as the 11:1 bandwidth Wilkinson divider/combiner presented here.

Since a Wilkinson divider requires resistors, in this work we demonstrate for the first time specially designed three dimensional surface mount pads for hybrid integration of 0402 and 0303 standard packaged resistors. This hybrid assembly method can be extended to other lumped passive and active components. The dividers utilize the available discrete values of surface-mount broadband resistors, and follow the constraints of the PolyStrata™ fabrication rules, which determine

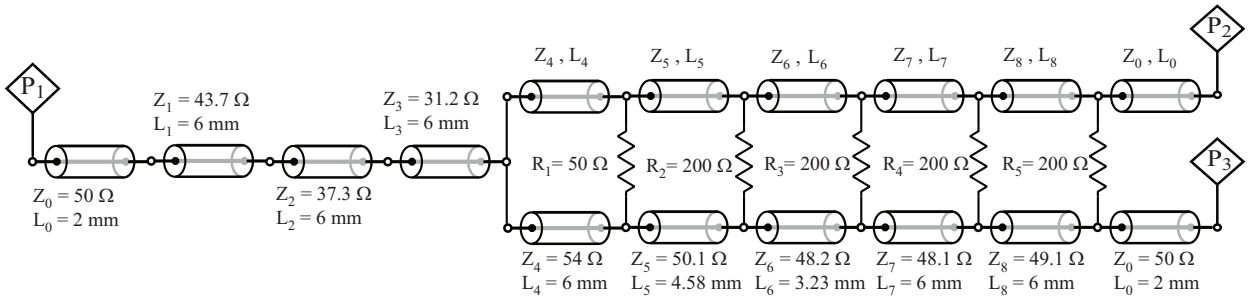


Fig. 2. Circuit schematic of the broadband Wilkinson divider with indicated characteristic impedances, lengths, and resistor values. This model consists of five pairs of transmission lines with five resistors between each pair. The input transmission line is composed of four sections.

the achievable characteristic impedances and the overall size of the circuit.

The paper is organized as follows:

- Section II details the design procedure and describes the fabrication process and its limitations. In particular, the circuit optimization process, as well as the full-wave electromagnetic simulation including hybrid resistors is presented. In addition, the miniaturization in terms of footprint reduction for a given coaxial line size is discussed;
- Section III presents the measured results on two versions of a smaller cross-section design, including a discussion on calibration using PolyStrata™ standards;
- The final two sections discuss unbalanced loads, power dissipation in the resistors, and possible extensions of this work to other types of dividers.

II. Fabrication and Design Procedure

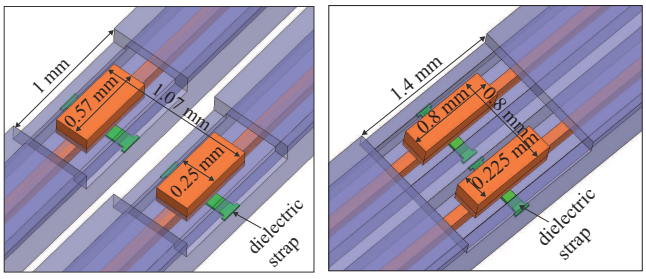
A. Fabrication

The PolyStrata™ process involves sequential deposition of copper layers and photoresist on a silicon wafer. Copper layer thickness ranges from 10 µm to 100 µm, with gap-to-height and width-to-height aspect ratios of 1:1.2 and 1:1.5, respectively. Fig. 1 (b) shows the cross-section of a five-layer 50 Ω micro-coaxial line, in which layers 1, 3, and 5 are 100 µm thick and layers 2 and 4 are 50 µm thick. The inner conductor is supported by 100 µm long dielectric straps with periodicity of 700 µm. After the desired layers have been deposited, the photoresist filling all space unoccupied by copper and dielectric straps is rinsed away ("released") through 200 µm × 200 µm release holes on layers 1, 2, 4, and 5, with 700 µm periodicity. Characteristic impedances available for a micro-coaxial line with this layer configuration range from 8 Ω to 54 Ω [14].

B. Design Procedure

As mentioned in Section I, a general broadband Wilkinson divider consists of M pairs of transmission lines with shunt resistors between them [3]. The number of sections, characteristic impedances, and resistor values determine the bandwidth. Since Cohn's basic design of a 50 Ω Wilkinson requires impedances greater than those available with the layer configuration shown in Fig. 1 (b), we chose to transform the input impedance of 50 Ω to a lower impedance at the point of the division. Port one is therefore composed of several sections of line with impedances varying from 50 Ω to approximately 30 Ω. A constraint of 54 Ω was placed on the maximum allowable impedance all transmission line sections in Fig. 2, and Ansoft Designer [15] was used to optimize the divider with $Z_0 = 50\,\Omega$ input and output ports. Fig. 2 shows the circuit model, in which the characteristic impedances and the lengths of the transmission lines are chosen from the results of the optimization process, and the resistors in between them are chosen based on the availability of resistor values in 0402 and 0303 packages. Due to the impedance constraint, six transmission line sections were required to achieve the desired return loss and isolation over the desired bandwidth.

The circuit from Fig. 2 was modeled in Ansoft High-Frequency Structure Simulator (HFSS) [16] for the five-layer process and in a straight geometry (unlike the reduced-footprint version shown in Fig. 1 (a)). The cross-sections of each transmission line section are calculated using the method from [13]. In order to place surface mount resistors in shunt between transmission line sections, 3D assembly pads, referred to as "passive sockets," are designed for both 0303 and 0402 standard packages, as shown in Fig. 3. The design of the passive sockets depends on the cross-sectional geometry of the transmission lines at the location where the socket is placed. If the field distribution is concentrated in the upper gap (layer 4), designing the sockets becomes more difficult due to field leakage from the open area of the outer conductor. Since the



(a) (b)

Fig. 3. Full-wave simulation model of two passive sockets designed for a shunt (a) 0402 and (b) 0303 chip resistor package. The lumped resistor is connected between the two pads; for (b) the two micro-coaxial lines share an outer conductor wall.

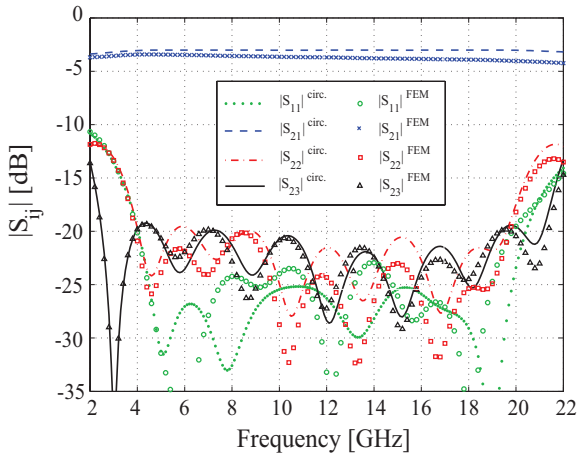


Fig. 4. FEM and circuit simulation comparison. $|S_{21}|^{\text{circ.}}$ and $|S_{21}|^{\text{FEM}}$ are -3.02 dB and -3.70 dB at 12 GHz respectively. Conductor losses are not taken into account for the circuit simulator.

fields were not very concentrated in the upper gap layer, there was not much difficulty in this design. This issue will be discussed in more detail for a divider with input and output ports of $12.5\,\Omega$ in Section V.

In the FEM simulation, the resistors are modeled as purely resistive impedance sheets. Fig. 4 shows the comparison between circuit simulations and the FEM results with the 0303 resistor packages. For the circuit model, ideal transmission lines and resistors are used; however, in the HFSS model, the conductor losses, as well as parasitics due to the "passive sockets" and resistors are taken into account, resulting in increased insertion loss. This device has a VSWR better than 2:1 from 2-22 GHz, and a better than 20 dB return loss and isolation from 4-18 GHz.

C. Miniaturization

In order to reduce the footprint of the straight Wilkinson divider, we miniaturized it by bending the transmission lines as shown in Fig. 1 (a). The length of the miniaturized divider is 18 mm, significantly less than the 48 mm long straight divider. This is facilitated by the high isolation between adjacent micro-coaxial lines [17] and judicious EM design of the tight bends. The difficulties encountered during the design of the miniaturized Wilkinson divider include maintaining the characteristic impedances of the transmission lines through the curves and careful design of the passive sockets.

III. Prototype Performance

Fig. 5 contains photographs of a fabricated straight Wilkinson divider, a passive socket for 0303 package surface mount component, and a miniaturized Wilkinson divider. The dividers were measured with an Agilent E8364B PNA four-port network analyzer, Cascade Microtech 250-µm pitch CPW microwave probes, and a Cascade Summit 9000 probe station. Two calibration methods were performed; the first was a three-port short-open-load-through (SOLT) implemented in CPW on an alumina substrate. This calibration method removes the effect of the cables and probes up to the probe tips. The straight Wilkinson divider was measured with this calibration method; Fig. 6 (a) and (b) show the comparison between s-parameter simulation and measurement results of this divider. One possible reason for the reduced performance in measured $|S_{23}|$ and $|S_{22}|$ above 16 GHz is imperfection in the manual mounting and positioning of the resistors in the sockets.

A broadband Wilkinson divider ideally has no amplitude or phase imbalance due to perfect symmetry [3]. In the actual circuit, however, due to fabrication imperfection the symmetry is broken and the measured amplitude and phase imbalance are calculated from

$$\Delta|S| = |S_{31}| - |S_{21}| \qquad [\text{dB}], \tag{1}$$

and

$$\Delta\phi = \angle S_{31} - \angle S_{21} \qquad [\text{deg}]. \tag{2}$$

Fig. 6 (c) shows the measured amplitude and phase imbalance of the straight Wilkinson divider. The phase imbalance is better than 1° and the amplitude imbalance is better than 0.1 dB.

The second calibration method is performed via an on-wafer PolyStrata™ TRL calibration standard, with two line standards to cover the full bandwidth. TRL calibration method removes the effect of the cables, probes, and probe to PolyStrata™ transition. The miniaturized Wilkinson divider was calibrated through this method; specifically, the divider was measured with the PNA using the three-port TRL calibration and three 250-µm pitch CPW microwave probes. Fig. 7 shows the comparison between simulated and measured results of the miniaturized Wilkinson divider. Measured amplitude and phase imbalance, from (1) and (2), are < 0.1 dB and $< 1^\circ$, respectively.

IV. Power Considerations

A. Effect of Mismatched Loads

In an ideal Wilkinson power divider, the current in the resistors is zero. However, this is not the case when there are slight mismatches at the output ports, or in the worst case, when a device or line at an output port fails as short or open. It is important to know how much current can flow through the resistors for specific mismatches, in order to select a resistor with appropriate power handling characteristics. Both the output port mismatches and the current flow in the resistor are investigated for the ideal broadband divider shown schematically in Fig. 2. Table I gives the RMS current in each resistor for different output port impedances ranging from $40\,\Omega$ to $60\,\Omega$, with 1 W of input power at 10 GHz. The maximum current in the resistors for $60\,\Omega$ and $40\,\Omega$ loads at the two ports is 4.71 mA, in $R_1 = 50\,\Omega$. Fig. 8 shows the simulated transient response of the current flow in each resistor for this case. The transient analysis was performed with a circuit simulator for 2 ns duration in 0.1 ps steps. Note that R_5 is the first resistor in which the current flows into, since this resistor is closest to the mismatched output ports. The selected 0402 (USMRG2040AN) and 0303 (USMRG3000AN) resistors can dissipate 3.45 W and 3.89 W, respectively, providing a significant safety margin.

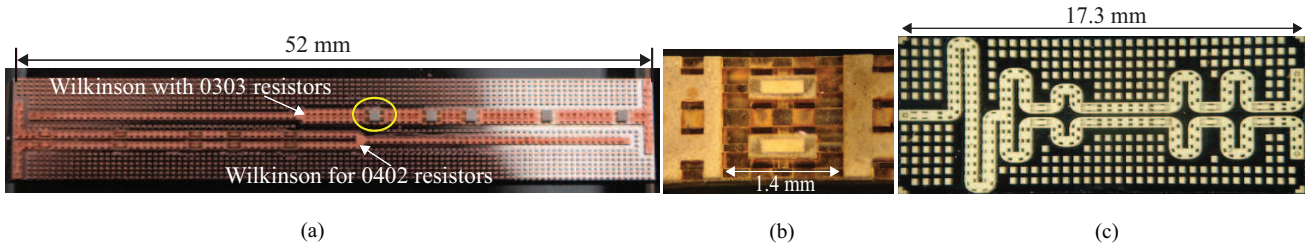


Fig. 5. (a) Photograph of the fabricated straight Wilkinson divider for both 0402 and 0303 sockets. Resistors are mounted on the divider with 0303 passive sockets. (b) Photograph of an 0303 passive socket with no resistor. (c) Photograph of the fabricated miniaturized Wilkinson divider.

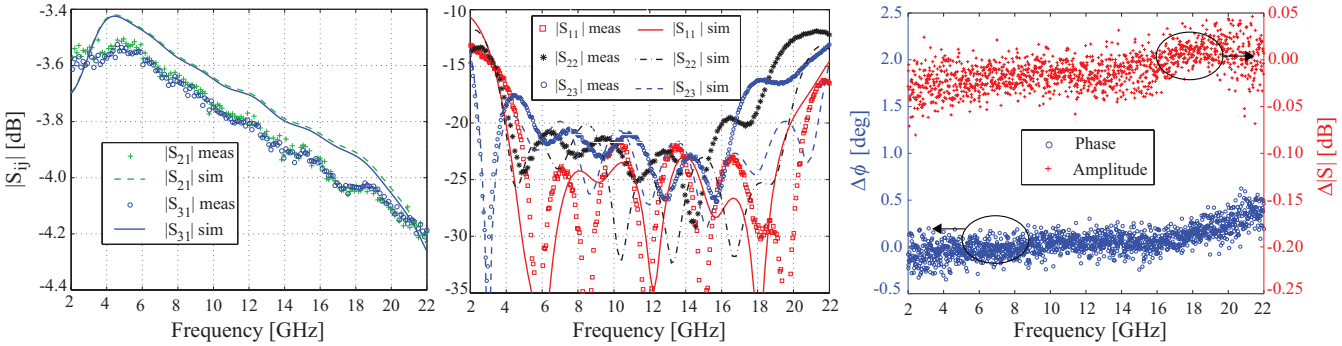


Fig. 6. (a) $|S_{21}|$ & $|S_{31}|$ and (b) return loss & isolation for the straight divider. (c) Measured phase and amplitude imbalance for straight divider; note that the scale covers 1° in phase and 0.1 dB in amplitude.

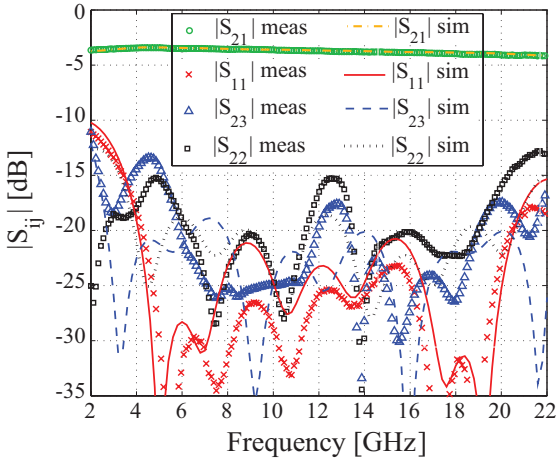


Fig. 7. Simulated and measured S-parameters results of the miniaturized Wilkinson divider with 0402 resistors. Measured $|S_{21}|$ at 12 GHz is −3.71 dB.

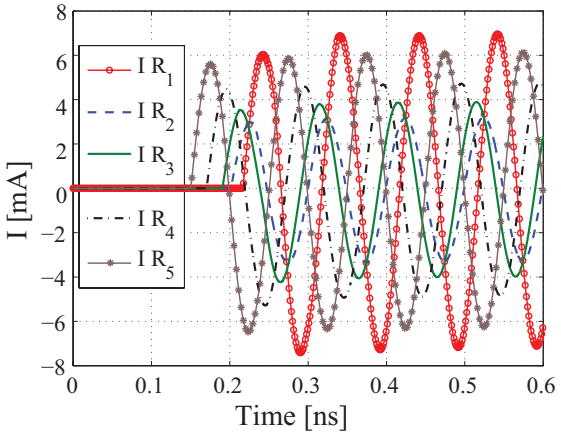


Fig. 8. Transient response simulation from $t = 0$ ns to $t = 0.6$ ns of current in each resistor. Ports 2 and 3 are connected to 40 Ω and 60 Ω loads, respectively. The analysis was performed for 2 ns duration with 0.1 ps steps.

B. RF Power Handling

The power handling capability of the dividers in this paper is limited primarily by the transmission lines' thermal and electrical breakdown limits [14]. Micro-coaxial lines with larger cross-sections allow greater power handling capability, increased design flexibility, and lower insertion loss. Fig. 9 (a) shows the cross-section of such a line, with eleven layers. The available characteristic impedances for micro-coaxial lines with the eleven-layer configuration range from 6 Ω to 140 Ω. A broadband miniaturized micro-coaxial Wilkinson divider was designed and fabricated with this larger cross-section line. Fig. 10 shows the circuit schematic of this divider, which consists of four parallel transmission lines and four resistors in the divider section, and three transmission lines sections in the input line; Table II shows their values. Although fewer transmission line sections are used in this design, the resulting bandwidth is still 2–22 GHz. This is due to the greater range of characteristic impedances available with the eleven-layer process compared to the five-layer line. This divider was modeled in HFSS and then fabricated in the PolyStrata™ process. Fig. 9 (b) and (c) show the simulated and measured results of this divider. Due to a process error that has subsequently been identified and corrected, the top layer,

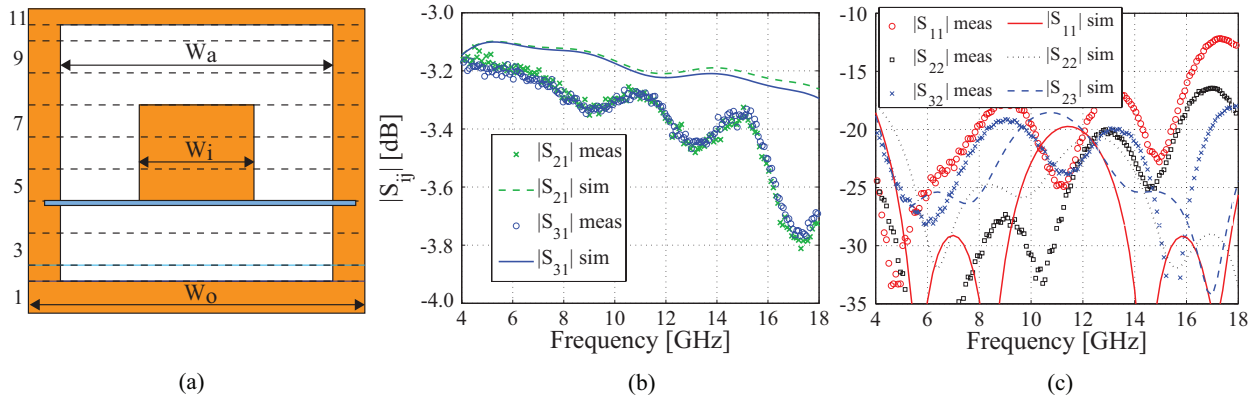


Fig. 9. (a) Cross-section of the eleven-layer micro-coaxial line; the height of layers 2, 10, and 11 is 50 µm; all other layers are 100 µm tall. $W_o = 1050$ µm, $W_a = 850$ µm and $W_i = 358$ µm are the dimensions for a 50 Ω with this cross-section (b) Simulated and measured $|S_{21}|$ and $|S_{31}|$ for the eleven-layer Wilkinson divider. (c) Return loss, isolation, and match at the output ports.

TABLE I
RMS CURRENT THROUGH RESISTORS FOR 1 W INPUT POWER AND VARIOUS LOAD MISMATCHES.

$R_{L(2,3)}$ [Ω]	40,50	45,50	40,55	45,55	40,60	45,60
I_{R1} [mA]	2.60	1.23	3.71	2.34	4.71	3.33
I_{R2} [mA]	1.19	0.56	1.71	1.08	2.17	1.54
I_{R3} [mA]	1.46	0.69	2.08	1.31	2.64	1.87
I_{R4} [mA]	1.79	0.85	2.56	1.61	3.25	2.30
I_{R5} [mA]	2.32	1.09	3.31	2.08	4.20	2.98

11, was not completely in intimate contact with the rest of the device. This seam was filled using conductive epoxy. Despite this problem, the transmission coefficient $|S_{21}|$ in the eleven-layer divider is approximately 0.4 dB better than the five-layer dividers due to the larger cross-section of the transmission lines.

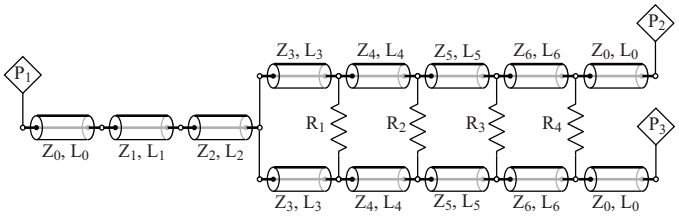


Fig. 10. Circuit schematic of the broadband Wilkinson divider designed for the eleven-layer process. The values of characteristic impedances, resistors and length of each sections are given in Table II.

TABLE II
ELEVEN-LAYER 50 Ω WILKINSON PARAMETERS

Section	0	1	2	3	4	5	6
Z [Ω]	50	46	41	70	66	61	55
l [mm]	1	6.3	6.3	5.4	4.0	5.1	5.8
R [Ω]	—	50	200	200	200	—	—

V. DISCUSSION

The implemented divider networks were all designed for 50 Ω ports. The intended application for this component is a miniaturized power combining broadband amplifier. Since active devices have low input and output impedances, it is advantageous to have the Wilkinson divider also perform partial impedance matching to the active device. Therefore, a broadband Wilkinson divider was designed in the eleven-layer PolyStrata™ configuration, with an input port impedance of 50 Ω and two 32 Ω output ports. The circuit schematic is the same as that of the eleven-layer divider in Section IV B and shown in Fig. 10. The characteristic impedances and lumped resistor values for this type of design are given in Table III.

TABLE III
ELEVEN-LAYER 50 Ω TO 32 Ω WILKINSON PARAMETERS

Section	0	1	2	3	4	5	6
Z [Ω]	50	44.7	37.3	59.3	48	42	37
l [mm]	1	6	6	5	3.8	5.3	5.2
R [Ω]	—	50	200	200	200	—	—

Another divider with low input and output impedances was designed for 12.5 Ω ports, in the eleven-layer PolyStrata™ process. The characteristic impedances selected for this divider are based on an optimization process and range from 12.5 Ω to 22 Ω, and the resistor values are 25 Ω, 50 Ω, 100 Ω, and 100 Ω. The input port consists of one section that is 12.5 Ω, unlike the other dividers in this paper. Since the characteristic impedances necessary for this divider are relatively low, the inner conductor height shown in Fig. 9 (a) is increased to 700 µm (layers 3 to 9). This can cause problems in the design of the passive sockets, since the electric field distribution is highly concentrated in the top (layer 10) and bottom (layer 2) gaps between the inner and outer conductors. In order to reduce the exposure of the electric field to the open areas of the passive sockets, the inner conductor is designed to be on layers 3 to 8 (i.e., vertically offset from the center), leaving a gap of 150 µm on the top between the inner and outer conductor. This causes

the electric field distribution to be concentrated in layer 2, and less concentrated between layers 9 and 10, making the structure suitable for implementing the sockets. Fig. 11 shows the electric field distribution for the two 12.5 Ω lines implemented in the eleven-layer configuration. This divider exhibits 2–22 GHz bandwidth, and its overall length after miniaturization is 14.5 mm. Fig. 12 shows a 3D rendering of the 12.5 Ω to 12.5 Ω divider without release holes and dielectric straps.

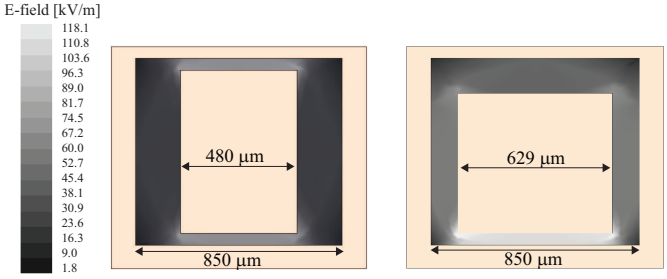


Fig. 11. Electric field distribution in 12.5 Ω lines in eleven-layer configuration for inner conductor height of (left) 700 µm and (right) 600 µm.

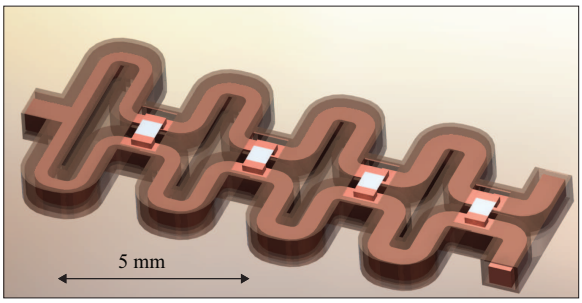


Fig. 12. Rendering of the miniaturized 12 Ω to 12 Ω Wilkinson divider implemented for the eleven-layer fabrication process. Release holes and straps are not shown in this figure. The outer conductor is rendered with 50 % transparency to show the inside of the divider.

VI. Conclusion

In summary, we demonstrated 11:1 bandwidth Wilkinson dividers implemented in micro-coaxial lines. Isolation between the output ports is better than 11 dB for 2–22 GHz, and the return loss is better than 13 dB over that range. Insertion loss varies from less than 0.2 dB at 4 GHz to 0.7 dB at 18 GHz, due to the increase from the skin effect loss in the copper. Several coaxial geometries for different power handling capabilities were considered. The power loss through the resistors was determined for ±20 % mismatch in the magnitude of the load impedances with at most 3.2 mW power dissipation in a 200 Ω resistor for 1 W of input power. The PolyStrata™ process enables hybrid integration of standard surface mount components which can be extended to active devices for a PolyStrata™ power combined amplifier. Alternatively, it is possible to detach the coaxial copper structure from the silicon substrate and integrate it with circuits made in different technologies.

Acknowledgment

This work is funded by the Defense Advanced Research Projects Agency (DARPA) DMT program, U.S. Army contract W15P7T-07-C-P437, and is approved for Public Release, Distribution Unlimited; DARPA case #13204, 3/16/09.

The authors would like to thank the Nuvotronics Microfabrication Team, Blacksburg, VA, and professor Dejan Filipović from the University of Colorado at Boulder.

References

[1] E. Wilkinson, "An N-way hybrid power divider," *Microwave Theory and Techniques, IRE Transactions on*, vol. 8, no. 1, pp. 116–118, 1960.

[2] J. R. Blodgett, "Power combiner/splitter," Jul. 1995. [Online]. Available: http://www.google.com/patents?hl=en&lr=&vid=USPAT5430418&id=T4EeAAAAEBAJ&oi=fnd

[3] S. B. Cohn, "A class of broadband three-port TEM-mode hybrids," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 19, no. 2, pp. 110–116, 1968.

[4] G. S. Makineni and W. T. Joines, "Comparison of the broadband performance of two-way power dividers and combiners," *Microwave and Optical Technology Letter*, vol. 17, no. 1, pp. 29–37, 1998.

[5] R. B. Ekinge, "A new method of synthesizing matched broad-band TEM-mode three-ports," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 19, no. 1, pp. 81–88, 1971.

[6] H. Oraizi and A. Sharifi, "Design and optimization of broadband asymmetrical multisection wilkinson power divider," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 5, pp. 2220–2231, 2006.

[7] Z. Popović, S. Rondineau, D. S. Filipović, D. Sherrer, C. Nichols, J. Rollin, and K. Vanhille, "An enabling new 3-D architecture for microwave components and systems," *Microwave Journal*, vol. 51, no. 2, pp. 66+, Feb. 2008.

[8] K. J. Vanhille, D. L. Fontaine, C. Nichols, D. S. Filipović, and Z. Popović, "Quasi-planar high-Q millimeter-wave resonators," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 6, pp. 2439–2446, 2006.

[9] K. Vanhille, D. S. Filipović, C. Nichols, D. Fontaine, W. Wilkins, E. Daniel, and Z. Popović, "Balanced Low-Loss Ka-Band µ-Coaxial hybrids," in *Microwave Symposium, 2007. IEEE/MTT-S International*, 2007, pp. 1157–1160.

[10] M. Lukić and D. Filipović, "Surface-Micromachined dual Ka-Band cavity backed patch antenna," *Antennas and Propagation, IEEE Transactions on*, vol. 55, no. 7, pp. 2107–2110, 2007.

[11] D. Filipović, M. Lukić, Y. Lee, and D. Fontaine, "Monolithic rectangular coaxial lines and resonators with embedded dielectric support," *Microwave and Wireless Components Letters, IEEE*, vol. 18, no. 11, pp. 740–742, 2008.

[12] K. Vanhille, "Design and characterization of microfabricated three-dimensional millimeter-wave components," Ph.D. dissertation, University of Colorado, 2007.

[13] M. Lukić, S. Rondineau, Z. Popović, and S. Filipović, "Modeling of realistic rectangular µ-coaxial lines," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 5, pp. 2068–2076, 2006.

[14] N. Ehsan, E. Cullen, K. Vanhille, D. Frey, S. Rondineau, R. Actis, S. Jessup, R. L. Jr., A. Immorlica, D. Nair, D. Filipović, and Z. Popović, "Micro-coaxial lines for active hybrid-monolithic circuits," *Microwave Symposium, 2009. IEEE/MTT-S International*, 2009.

[15] A. Corporation, "Ansoft designer." [Online]. Available: http://www.ansoft.com/products/hf/ansoft_designer/

[16] ——, "High frequency structure simulator." [Online]. Available: http://ansoft.com/hfss/

[17] Y. Saito and D. Filipović, "Analysis and design of monolithic rectangular coaxial lines for minimum coupling," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 55, no. 12, pp. 2521–2530, 2007.