Single Clock Control Logic Block (CLB) design for a QWIP-FPA ROIC

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***Abstract* — A Control Logic Block (CLB) of a Readout Integrated Circuit for a Quantum-Well Infrared Photodetector Focal Plane Array (QWIP-FPA ROIC) is designed and simulated. Through the use of a single input signal (CLOCK), it can be generated up to twelve synchronized control signals for the management of all QWIP-FPA functions and its interface with the external devices. The results indicate better performance than the available devices, which use up to seven external CLOCKS that must be synchronized, inserting extra difficulties in the project. Through an easy implemented topology, designed in VHDL, it is possible to control a 64 cells FPA prototype (8X8 Matrix). Few modifications are required to use this circuit with bigger FPAs.**

***Key-words* —VHDL, control logic block, digital design.**

I. INTRODUCTION

Since the 50's, technology dedicated to infrared systems has been developed for different applications. Astronomy, medical imagery and electronic industry are examples of the most benefited areas. These areas are responsible for a great part of the recent IR systems development. [1-5]

On the other hand, the military area has been using infrared detection in different applications such as smart weapons, search and track, mine detection and others [6].

Process improvements and the development of microelectronics in the last twenty years have increased the size and performance of detectors, which are known as Focal Plane Arrays (FPA). These FPA are composed essentially by two parts: the photodetector and the readout.

In Instituto Tecnológico de Aeronáutica (ITA), specially in the Electronic Warfare Lab, there is a research area where QWIPs are being fabricated as well as the first ROIC unit cells. The ability to operate several unit cells together as readout of a camera requires an architecture that provides the logic control and the integration of the different FPA modules. This is the main objective of this paper, where a Control Logic Block (CLB) is designed and simulated. The main idea is to use a single CLOCK signal to generate until twelve signals to manage the ROIC functions and the output interface with external devices. Similar devices like this use until seven CLOCK signals [7-9] with the additional need of external signal synchronization, requiring extra power.

The purpose of this design is to proof a concept that could be applied in bigger FPAs.

II. ROIC ARCHITECTURE

A dedicated ROIC design is made by combining analog and digital circuits. The difficulty level increases when both have to operate together. The points where these signals interface each other are always complex and sources of additional noise.

Fig.1 shows a block diagram of the ROIC architecture, with the different component modules. The analogical ones (BIAS Control, line and column selectors, main matrix and output buffers) are responsible for the basic ROIC functions of selecting the pixel, read, amplify, and make the signal available to an external device, serially. On the other hand, there is an important digital block named "control logic" responsible to generate adequate signals to control all the analogical ones.

In this work, preliminary studies to design a complete ROIC are performed. To do that readout configuration, a small detector matrix (8x8) is proposed, aiming to reduce noise, frequency of operation and increase transimpedance gain.

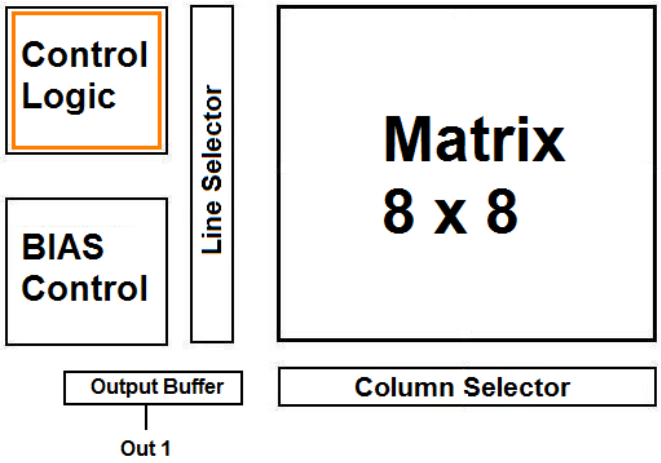

Fig. 1. ROIC Block diagram.

The modules that need temporization control are the selectors (column and line selectors) and the unit cells (inside the matrix), that will perform the integration and the reset of the input signal.

In order to design the temporization CLOCKs, the requisites of the device must be considered. First of all, the intended frame rate, about 240 fr/s, is enough to be highly above the detection of human eyes and optimal for military

imaging. This provides a frame period of 4.16ms. Considering the ROIC of the Fig. 1, each one of the 8 lines have to be selected at a time, what reduces the period to 520µs for each line. In this period the circuit has to be able to integrate and read the signal (Integrate then read signal processing - ITR). This method demands a lower reading frequency, however can be implemented in an easier way. As the matrix is composed of only 64 pixels and was idealized as a proof of concept, the operational frequency is not a restrictive parameter. Operating with a 50% of duty cycle in this CLOCK, it is possible to achieve the necessary integration time of 260µs with an equal sampling time.

After establish these requisites, the necessary temporization could be obtained through a fundamental reference CLOCK of 2µs. This will provide all other temporization signals as multiples of the fundamental one as listed below:

- line selector signals of 1024, 2048 and 4096µs period "line [0,1,2]", defining each one of the 8 lines;
- column selector signal of 64, 128 and 256µs period "sel [0,1,2]", defining each one of the 8 columns, active only during the sampling period;
- integration/sampling signal of 512µs period with a 50% duty cycle "Vint", where the low level integrates the signal and the high level samples it ;
- a reset signal with 512µs period and a duty cycle of 2µs "Vreset", active before each integration period, in order to reset the frame signal and avoiding cross-talk; and
- a signal that will be used to reset output buffer between each sampling signal "Vnul", with a period of 32µs and a duty cycle of 2µs, active only during the sampling period.

The time chart describing all the signals above mentioned can be seen in Fig.4, after simulating the proposed circuit.

On the other hand, more signals are necessary in order to realize the interface with an external device, which can be a video screen or an ADC. These output indicators are:

- First column of the matrix indicator "column1a", signing that a new line is beginning;
- First line of the matrix indicator "line1a", signing that a new frame is beginning; and
- First pixel of the matrix indicator "referencia", signing the reference pixel to a video layout presentation and that a new frame is beginning.

The existence of these signals refers to the faithful reproduction of the image through any chosen interface. References are always checkpoints to the post-processors and necessary for the image reconstruction.

III. BLOCK DESIGN

In order to develop a circuit able to generate all the signals above mentioned, it was used a combination of tools from the software Mentor Graphics and from software Cadence. The multi-software approach is justified by the features provided by each tool.

As a digital design, the device was first implemented in VHDL and post-transformed in Verilog language, in order to become easier to interface with Mentor Graphics. The compilation and simulation as digital cells are easier than using an analogical low level approach.

After defining all the necessary output signals, a pre-design was made with FPGA Advantage, from Mentor Graphics. Through a schematic design, the cells of a foundry were instanced and simulations were performed to have a first approach of device behavior. No cell delays were implemented at this phase of the project. Once finished the circuit and the behavior agreed with the desired one, it was implemented in VHDL language.

The code was done in 225 lines and can be easily modified to support different levels and sizes of matrix (FPA). The architecture uses basically flip-flops, counters, and logic gates.

The VHDL code was converted in Verilog language using Cadence Encouter RTL Compiler. With this software it was possible to convert the code to verilog and have an idea of the circuit compiled in basic cells. At this point, a simulation could be performed with more realistic characteristics of the basic cells. All the delays of the circuit were analyzed. In order to minimize consequent problems of the cells delays, it was defined a synchronized topology for the device, where only the reset signal "Vreset" presented some level of delay, which does not compromise the performance of the ROIC.

In the schematic diagram generated by RTL Compiler through the Verilog input, seen in Fig.2, it is possible to verify a single CLOCK signal generating all the twelve output proposed signals. It is important to know that only basic digital cells were used at this phase of the project, becoming easily the implementation of this architecture through silicon or a FPGA Development kit.

As the intention of this design is implement the topology embedded in an integrated circuit, the next necessary step is making the design layout into silicon, what was done through software Mentor Graphics.

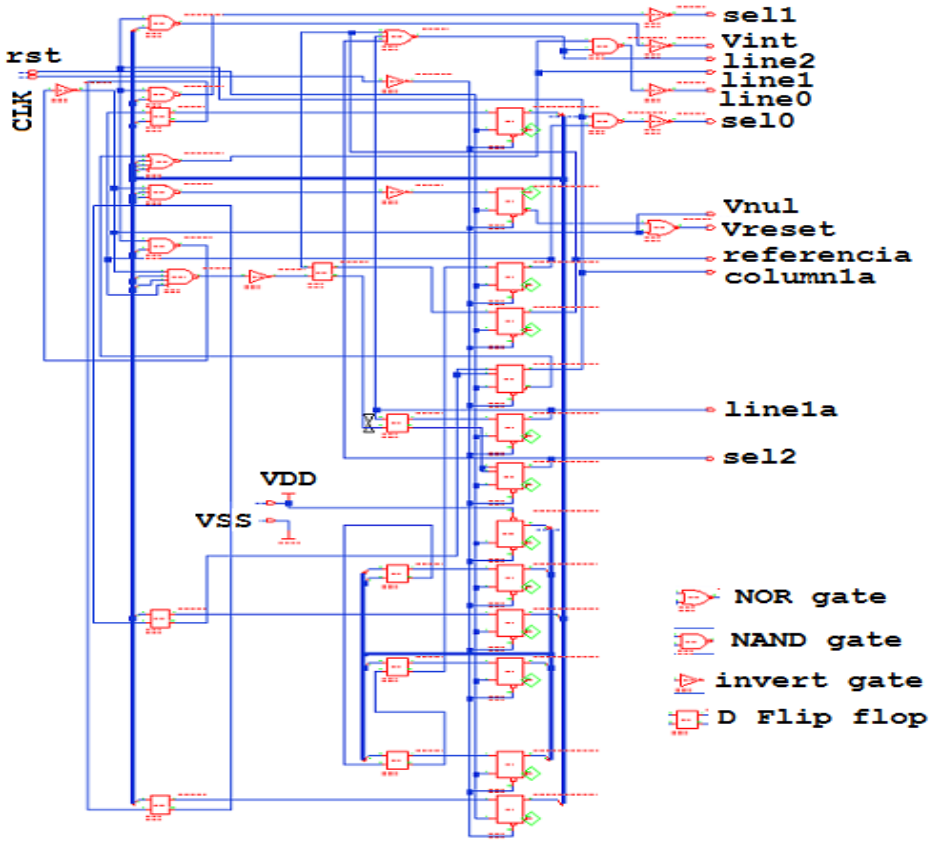

Fig. 2. Schematic diagram with basic cells from Design Architect, in IC Studio, by Mentor Graphics

The simulations were performed in high level, using a specific viewpoint level of Mentor Graphics called "cell" designed to digital cells simulations. This approach makes the simulations faster and more adequate to digital circuits.

IV. SIMULATION RESULTS

Fig.3 shows the Test Bench created to analyze the circuit performance.

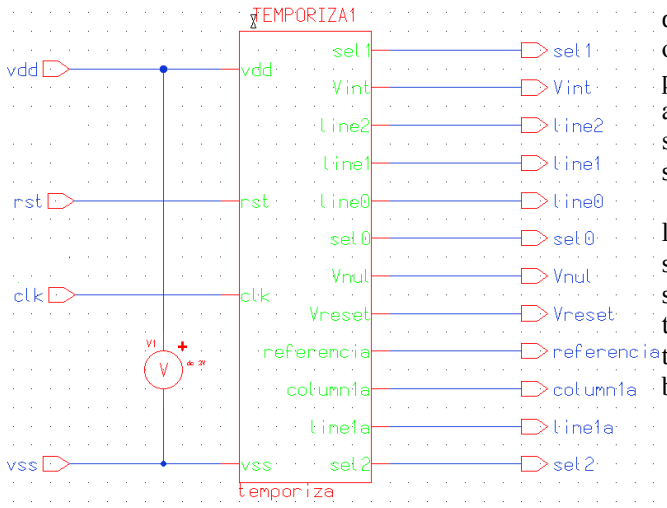

Fig. 3. Generated Test Bench through Design Architect, in IC Studio, by Mentor Graphics

In Fig. 3 it can be seen the input signals (clk and rst), the power signals (vdd and vss) and the output signals. The "rst signal" is necessary in the beginning of the operation in order to avoid "undetermined states".

A 4.5ms simulation period was run in order to sweep a full frame period and to validate the block outputs.The simulated results of the final architecture can be seen in Fig. 4. It is possible to verify the agreement between the proposed signals and the implemented ones.

The transitions are always synchronized, what makes the device independent of delays between the cells and the outputs. Three bits of line selector "line[1…3]" make possible a top-down sweep of the FPA, showing, in each line, a complete "Vint" period, allowing an "integration then read signal processing" of all the pixels in a same line, simultaneously.

The signals "sel[0…2]" are activated only during high level signal of the Vint, making possible the sampling of the signal after its integration and freezing by a sample and hold structure. In order to reset the signal between one sample and the next, it was implemented the "Vnul" signal just before transition of each sampling signal to the next state. This behavior is better observed in Fig. 5.

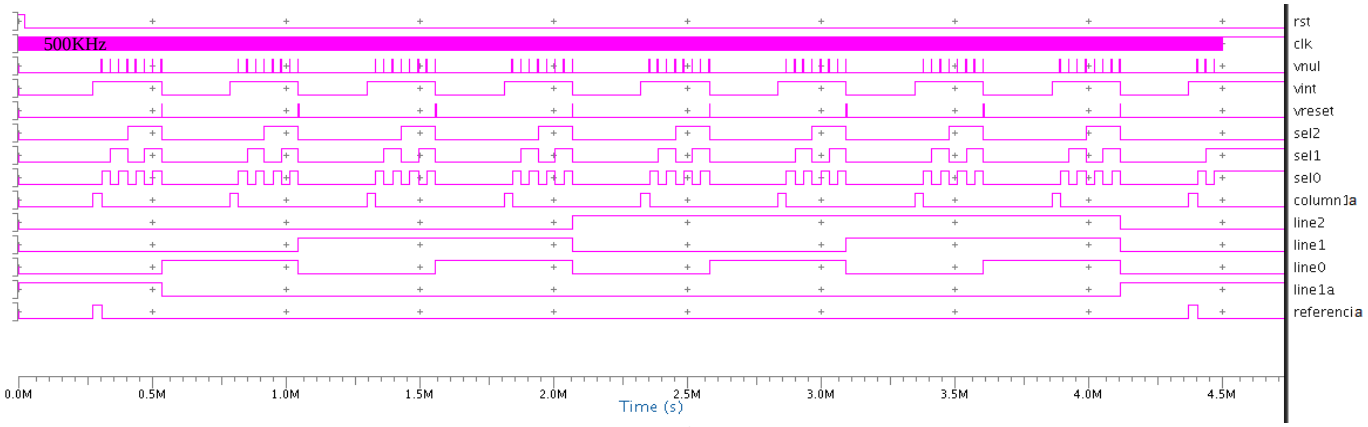

Fig. 4. Input and Output signals of the Control Logic Block (CLB).

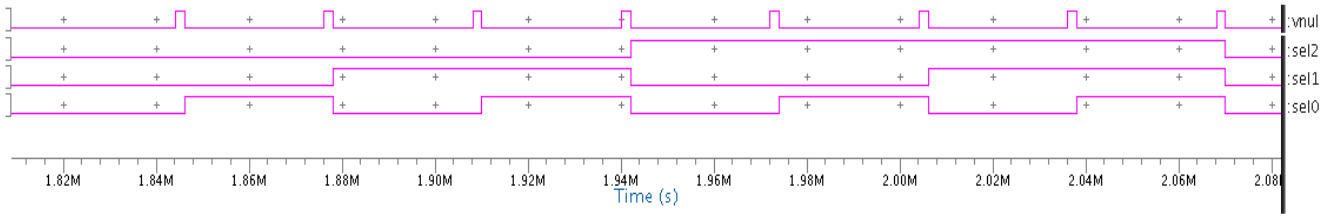

Fig. 5. Temporization signals for the sampling period of the Control Logic Block (CLB).

The signal "Vreset" is active just before every integration period (low level of Vint), nulling the charges and avoiding cross-talk between frames.

At the same way, all the interface signals (column1a, line1a, referencia) are present and synchronized with the others before mentioned.

Therefore, it is possible to conclude that the circuit complies with the requisites and is a good approach to be implemented. The layout design was made using Mentor Graphics, applying the automatic instance tool, in order to obtain a bigger density of gates. The circuit is ready to be fabricated and its characterization is a matter for future work. It is possible to see, in Fig. 6, the final layout of the proposed block.

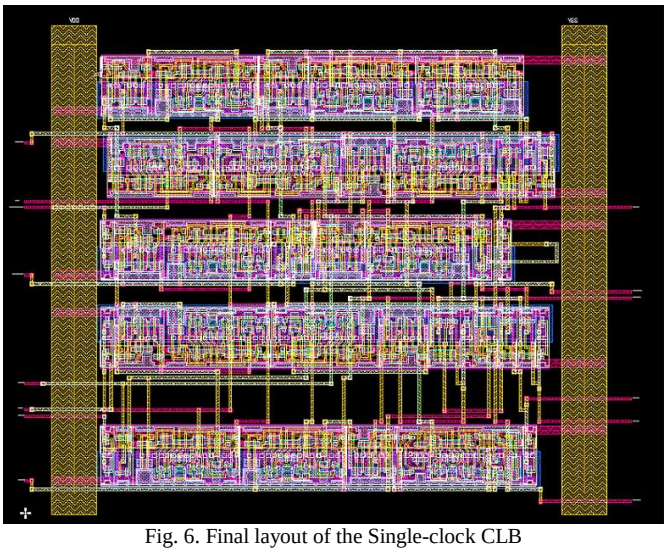

Fig. 6. Final layout of the Single-clock CLB

V. CONCLUDING REMARKS

A full Control Logic Block (CLB) design was demonstrated in order to generate the signals of a FPA 8x8, being a first approach to bigger matrix. Simulation results have shown that a full synchronized control signal set can be generated by CLB, avoiding the necessity of external synchronization, what minimize area and power dissipation, once it does not need other circuits to do the cells signal synchronization. The CLB works based in only one input CLOCK signal, being able to generate twelve ones. This result indicates an improvement of the current available ROICs where up to seven inputs are needed. This feature allows saving input PADs, external signal generators, external synchronization devices, area and power dissipation. Furthermore, this configuration can be easily adapted to be used with bigger FPA, requiring just small changes in the VHDL code. In addition, it is possible to include some extra ROIC functions, such as windowing, reverse read mode, etc. The fabrication and characterization is a matter of future work.

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REFERENCES

[1] R. J. Dempsey, D. G. Davis, R. G. Jr. Buice, R. A. Lodder, "Biological and medical applications of near infrared spectrometry," Appl. Spectr., vol. 50, no. 2, p. 18A–34A, Fevereiro. 1996.

[2] N. Itoh, K. Yanagisawa, T. Ichikawa, K. Tarusawa, H. Kataza, "Kiso observatory near-infrared camera with a large format array," in Proc. SPIE, Infrared Technology XXI, 1995, vol. 2552, p. 430–437.

[3] D. C. Murphy, S. E. Persson, M. A. Pahre, A. Sivaramakrishnan, S. G. Djorgovski, "An infrared camera for the Palomar Observatory 60- inch

telescope," Publications Astronomical Soc. of the Pacific, vol. 107, p. 1234–1242, 1995.

[4] D. A. Scribner, M. R. Kruer, J. M. Killiany, "Infrared focal-plane array technology," Proc. IEEE, vol. 79, no. 1, p. 66–85, 1991.

[5] E. R. Fossum, B. Pain, "Infrared readout electronics for space science sensors: State of the art and future directions," in Infrared Technology XIX, Proc. SPIE 2020, 1993, p. 262–285.

[6] BUNDAS, J, et al. Two-color quantum well infrared photodetector focal plane arrays. **SPIE 6206-16**, v.1, p.1-11, março. 2006.

[7] ISC 9705 Standard 320 Specification 400-9705-09 Version 1.3. Disponível em: http://www.imrex.com.sg/productDoc/9705spec.pdf. Acesso em: 15 de março de 2010.

[8] ISC 9802 Linear 512 Specification 400-9802-09 Version 110. Disponível em: http://www.imrex.com.sg/productDoc/9802spec.pdf. Acesso em: 15 de março de 2010.

[9] ISC 0002 Specification and requirements review. Disponível em: http://www.imrex.com.sg/productDoc/0002spec.pdf. Acesso em: 15 de março de 2010.