Design of Minimum Circuit for Interval Type-2 Fuzzy Logic Controllers Applications

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***Abstract* – Most applications involving real world systems faces with uncertainties that are difficult to predict. These uncertainties can be associated to the changes in their operational conditions due to varying load and environmental conditions. The main advantage of type-2 Fuzzy Logic is that it can handle with uncertainties. This paper presents the design of a new current-mode CMOS minimum circuit that are used to perform the inference process of the type-2 fuzzy controller chip. The proposed circuit will be compared with Yamakawa´s minimum circuit and its main parameters discussed. The circuit was designed and simulated in 0.35µm CMOS technology with 3.3 V power supply. The simulation results verified the function and accuracy of the minimum circuit.**

***Keywords* — Type-2 fuzzy logic controller, Minimum circuit, Analog circuits.**

I. INTRODUCTION

The type-2 fuzzy controllers have been used in a large number of applications because it can handle with uncertainties more effectively than type-1 fuzzy sets [1-3]. An application example of type-2 fuzzy controller in military area is the control of the Unmanned Aerial Vehicle (UAVs) [4]. The main problem in the development of UAVs is the operation environment that contains a significant level of uncertainties. In this work [4] the author has compared the performance of type-1 and type-2 fuzzy controller, showing the superiority of type-2 fuzzy controller for uncertainties applications.

This paper presents a new circuit for the minimum loser-take-all operation. Minimum circuit has a wide range of applications in analog fuzzy logic controllers and artificial neural network [5-10]. This paper proposes a minimum circuit applied to a type-2 fuzzy logic controller chip.

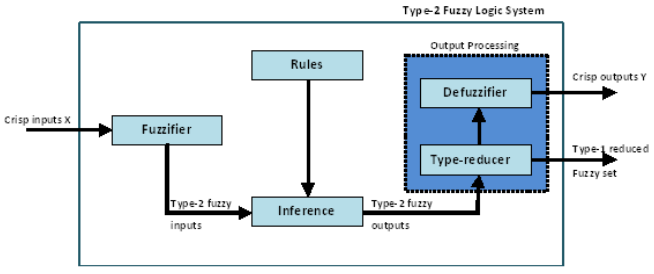

Fig.1. Structure of Type-2 fuzzy logic controller.

The type-2 fuzzy logic controller (Fig. 1) consists of a fuzzifier, an inference process, a rule base, a type-reducer, and a defuzzifier [11]. The fuzzifier converts the crisp inputs into a type-2 fuzzy set. In the inference engine block, the type-2 fuzzy set activates the rule base to generate the output type-2 fuzzy sets. The type-reducer converts an interval type-2 fuzzy set into a type-1 fuzzy set. The defuzzifier produces the crisp output.

The type-2 fuzzy controller is composed by type-2 fuzzy sets. As presented in Fig. 2a, in type-1 fuzzy set the membership grade for each element is a crisp number. The membership function (MF) of type-2 fuzzy set has a footprint of uncertainty (FOU). The secondary MF of type-2 fuzzy sets can be uniform or non-uniform, as shown is Fig. 2b.

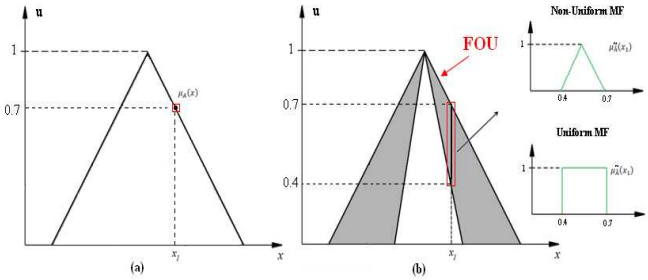

Fig. 2. Membership function (a) Type-1fuzzy set (b) Type-2 fuzzy set.

The uniform secondary membership function is called Interval type-2 fuzzy sets. It is used to reduce the computational complexity of type-2 fuzzy sets [11-12].

The FOU of type-2 fuzzy set is bounded by an upper and lower type-1 membership function denoted by: $\overline{\mu_F}$ and $\underline{\mu_F}$ respectively [11]. The Fig. 3 shows a type-2 inference system for a rule that has two antecedents and one consequent for the following rule: *IF* x_1 *is* F_1 *and* x_2 *is* F_2 *THEN y is G.* The membership function of the antecedent x_1 is activated by x_1' and produces an upper and lower activation degree at x_1'. The activation degrees of the antecedent x_2 are obtained in the same way. The minimum of the upper and lower activation degrees are taken, producing the upper ($\overline{f}$) and lower ($\underline{f}$) activation level.

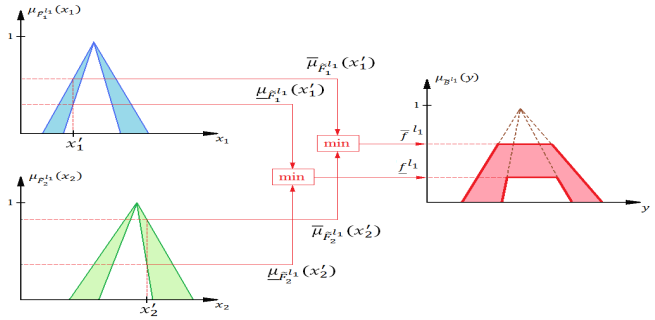

Fig. 3. : Type-2 Fuzzy Logic Inference for one rule.

In this work we propose a structure of minimum circuit based on Wilson current mirror. The minimum circuit has two inputs and one output, as shown in type-2 fuzzy inference diagram (Fig. 3). The main advantages of the proposed circuit are small die area, high accuracy and output resistance higher than the circuit proposed by Yamakawa [9].

This paper is divided in the following sections: section 2 presents the minimum circuit proposed. The section 3 presents the device simulation results, and finally, in section 4 the conclusions of the work are presented.

II. PROPOSED MINIMUM CIRCUIT

The current-mode minimum circuit (Fig. 4) was proposed by Yamakawa [9]. This circuit is expressed by bounded-difference, which is a fundamental fuzzy logic function.

$$I_{OUT} = MIN(I_X, I_Y) = I_X \Theta (I_X \Theta I_Y) \quad (1)$$

where: $$I_X \Theta I_Y = \begin{cases} I_X - I_Y & \text{se } I_X > I_Y \\ 0 & \text{se } I_X < I_Y \end{cases}$$

The bounded-difference can be implemented with current mirrors and MOS transistor connected as diode. As example, consider that $I_y > I_x$. In this case, the current I_x will be drained by transistor M_2, and therefore the current in both transistor M_3 and M_4 will be null. Then, the output current, I_{out}, is given by I_x. If $I_x > I_y$, the current I_y will be mirrored to the transistor M_2, and the current in both transistor M_3 and M_4 will be $I_x - I_y$. Then, the output current, I_{out}, is given by $I_y = [I_x – (I_x - I_y)]$, that represents the lowest current injected in the circuit.

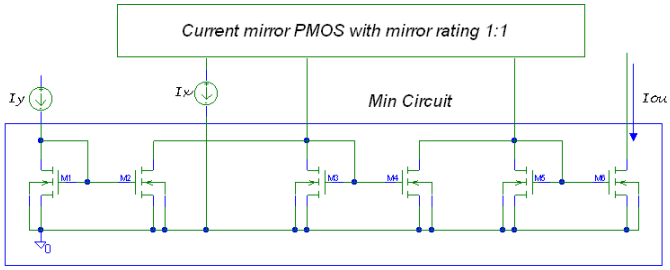

Fig. 4. Minimum circuit proposed by Yamakawa [9]

The Yamakawa´s minimum circuit (Fig. 4) was implemented based on simple current mirror. The main problem of this circuit is the accuracy. Due to the channel length modulation λ and the difference of drain-source voltage of the transistors M_1 and M_2, the output voltage has an accuracy error [13]. This accuracy error of simple current mirror can be explained by the expression below:

$$\frac{I_2}{I_1} = \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \quad (2)$$

This accuracy error also happens in the second (M_3 and M_4) and third current mirrors (M_5 and M_6) and is accumulative. In addition, this circuit presents a low output resistance given by: $1/\lambda I_{out}$.

In order to solve this problem, this paper proposes a different topology. As the current that flow in the transistor M_2, is the minimum current, it was possible to use a Wilson current mirror, which has good accuracy to mirror this current to the output.

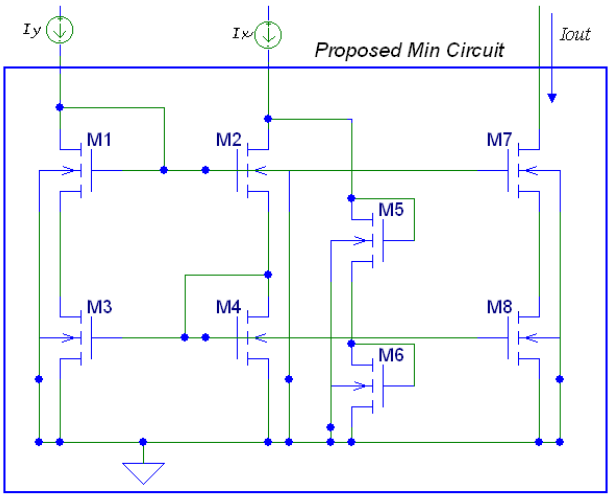

Fig. 5. The proposed minimum circuit.

The Fig. 5 shows the proposed minimum circuit. The current of transistors M_2 and M_4 is always the minimum current and it is mirrored to the output. If $I_y > I_x$, the current I_x will be drained by transistor M_2 and M_4, as a consequence the current in both transistors M_5 and M_6 will be null. Then, I_x current will be mirrored to the output current, I_{out}. If $I_x > I_y$, the current I_y will be mirrored to the transistors M_2 and M_4, and the current in both transistor M_5 and M_6 will be $I_x - I_y$. Then, the output current, I_{out}, is given by the mirrored current I_y. The output resistance of the proposed circuit is expressed as:

$$R_{out} \cong r_{ds7} (g_{m7} r_{ds8}) \quad (3)$$

The output resistance of the proposed circuit is higher than the output resistance of Yamakawa´s circuit. With higher output resistance, the load effect of the proposed circuit is minimized.

III. SIMULATION RESULTS

The operation of the minimum circuit has been simulated using Mentor Graphics simulator and 0.35µm AMS model. The dimensions of this transistor were calculated based on the AMS model and the nominal current of 10µA.

The Fig. 6 shows the first simulation result of proposed minimum circuit. The current I_x has a constant value 10µA and I_{out} is the minimum current between the currents I_x and I_y. The output error is 1,3nA which results a dynamic behavior with accuracy of 99,9%.

The Fig. 7 shows the second simulation of minimum circuit. In this case the input current I_x is a sinusoidal signal with amplitude of 5µA, DC offset of 5µA and frequency of 0.5 kHz. The minimum output of I_x and I_y is shown in Fig. 7. The two tests verified the functionality of the proposed

minimum circuit and both simulations presented high accuracy (99,9%).

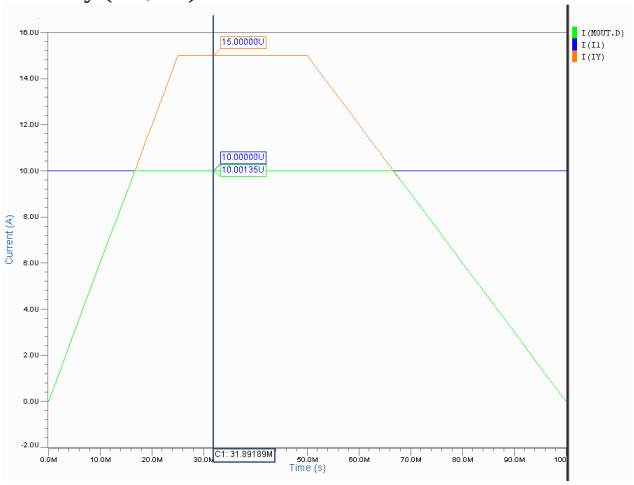

Fig. 6. First simulation result of the proposed minimum circuit.

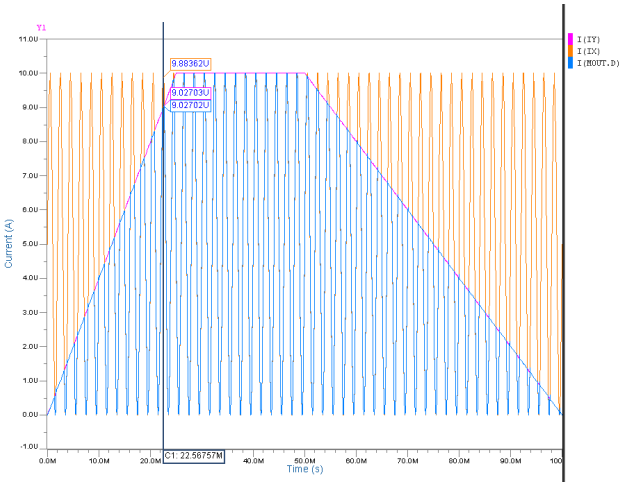

Fig. 7. Second simulation result of the proposed Minimum circuit

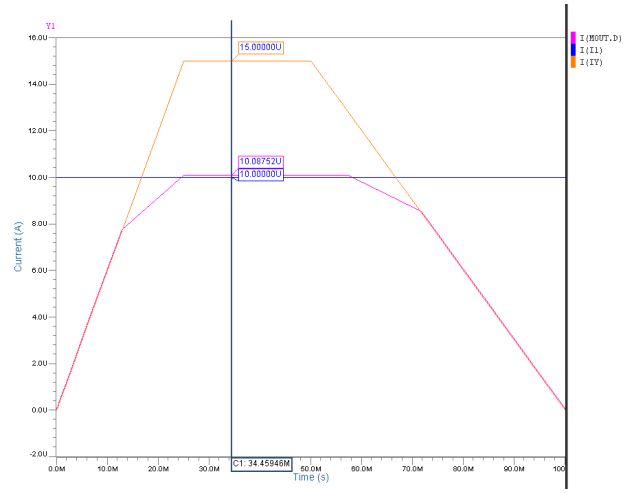

Fig. 8. Simulation result of Yamakawa´s Minimum circuit.

In order to compare our proposed circuit with the Yamakawa´s minimum topology, the second was simulated using the same technology and parameters of the previous one. The dimensions of this transistor were calculated based on the AMS 0.35µm model and the nominal current of 10µA.

The Fig. 8 shows the simulation result of Yamakawa´s circuit for I_x equal 10µA.

The I_{out} current of Yamakawa´s minimum circuit has presented a discrimination error. This error is given by the difference between the smaller current (I_x) and the actual output current I_{out} [13].

IV. CONCLUSIONS

This paper proposed a new current-mode two input one output minimum circuit designed in 0.35µm CMOS technology. Compared with Yamakawa´s circuit, the proposed minimum circuit has the following advantages:

-Higher output resistance: The output resistance of the proposed circuit is between 10 and 100 times higher than of the previous circuit. The high output resistance reduces the load effect.

- High accuracy: the main cell of the proposed minimum circuit is the Wilson current-mirror, this current mirror reduces the difference of drain-source voltage, so the discrimination error caused by the channel length modulation λ is reduced. The accuracy of the proposed circuit (99,9%) is 10 times higher than the Yamakawa´s circuit simulated with the same technology and parameters of the proposed circuit and despising the discrimination error.

Through the circuit simulation results obtained, in AMS CMOS 0.35µm technology, it was observed the functionality of minimum circuit. In addition the simulation shows that it can be very useful as t-norm minimum inference circuit in the type-2 fuzzy controller chip.

REFERENCES

[1] H. Hagras, "Type-2 FLCs: A new Generation of Fuzzy Controllers," IEEE Computational Intelligence Magazine, vol. 2, N. 1, p. 30-43, Fevereiro, 2007.

[2] J. M. Mendel, “Uncertain Rule-Based Fuzzy Logic Systems: Introduction and New Directions”, Prentice-Hall, Upper-Saddle River, NJ, 2001.

[3] O. Castillo, P. Melin, “Type-2 Fuzzy Logic Theory and Applications”, Springer-Verlag, Berlin, 2008

[4] C. Lemire, “Unmanned Aerial Vehicle trajectory tracking using Type-2 Fuzzy Logic”, Dissertation, Royal Military College of Canada , 2008.

[5] M. Rahman, K. L. Baishnab, F. A. Talukdar, “A High Precision VLSI Loser-Take-All Circuit for Neural Networks and Fuzzy Systems”, IEEE Int. Conference on Computational Intelligence for Measurement Systems and Applications, Hong Kong, China, Maio 2009.

[6] B. Mesgarzadeh , “A CMOS Implementation of Current-Mode Min-Max Circuits and A Sample Fuzzy Application”, IEEE, Julho 2004.

[7] G. Yosefi, S. Mirzakouchaki, S. Neda, “Design of new CMOS current mode Min and Max circuits for FLC chip applications”, IEEE, 2009.

[8] V. F, Dinavari *et al*, “Design of a current-mode analog CMOS fuzzy logic controller”, IEEE, 2009, p. 211-217.

[9] T. Yamakawa, T. Miki, F. Ueno. “The design and fabrication of the current mode fuzzy logic semi-custom IC in the standard CMOS IC technology,” in Proc. 15th IEEE Symp. Multiple valued Logic, Maio 1985, p. 76-82.

[10] M. Sasaki *et al*, “Fuzzy Multiple input maximum and minimum circuits in current mode and their analyses using bounded-difference equations”, IEEE Trans. , vol. 39, No 6, Junho 1990, p. 768-774.

[11] J. Mendel, "Type-2 fuzzy sets and Systems: An Overview," IEEE Computational Intelligence Magazine, p. 21-29, Fevereiro 2007.

[12] J. Mendel, R. John "Type-2 fuzzy sets made simple," IEEE Transactions on Fuzzy Systems, vol. 10, p. 117-127, Abril 2002.

[13] J. Baker, “CMOS Circuit Design Layout and Simulation”, IEEE Press, Second edition, 2007.