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A CMOS 0.18µm 4bits PROGRAMMABLE DELAY CONTROL FOR UWB TIMED ARRAY BEAMFORMING RADAR APPLICATION

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ABSTRACT. We present a Programmable Delay Control (PDC) for UWB Timed Array Radar Application, working with pulses in the GHz region, which requires a precise control of delays in the order of picoseconds. The major component of the PDC consists of a channel formed by two static inverters connected in series. Between the internal transition line (V_{linha}) and the ground line (*Vss*), a digital variable capacitor is used to control the time of transitions (low-to-high and high-to-low) through their different times of charging and discharging. The circuits are designed using the integrated Spice environment with MicroWind 3 and LTSpice 4 VLSI Full custom project tools with the IBM SiGe 0.18 um process foundry. The Spice simulations showed a controllable delay time between 0 and 97ps, which, in the EM tests with CST Microwave Studio 2011, resulted in a controlled beam with center frequency of 4GHz, angular width of 27 ° and variable deflection between 12 º and -13 º, with a 8.3dB directivity and sidelobe of-11dB.

Keywords: **Delay Control, UWB Radar, Timed Array.**

I. INTRODUCTION

Programmable delay controllers (PDC) are usually characterized to modify the rise and fall times of digital signals or other transition signals in integrated circuits (IC). In a PDC, the delay between input and output can be controlled digitally or analogically. In the analogic form, delay can be regulated by varying an analog control voltage, which allows a continuous adjustment of delay time [1]. In the digital form, delay can be regulated by discrete voltage levels [2] or discrete variation of a capacitance [3].

There are various applications for PDC circuits, e.g. in digitally controlled oscillator circuits [2], Phase-Loched Loops (PLL) circuits [4], Delay-locked Loops circuits [5], and high performance CMOS VLSI circuits, such as microprocessors and dynamic memories [6]. In all those applications, the PDC is an essential component and its accuracy directly affects the circuit performance [7].

De Oliveira *et. al* [8] has proposed the use of PDC to manage delay signals of stimulation, in the configuration of radar-Timed Array Transmitter. This allows controlling the beam direction without mechanical movement in an antenna. Figure 1 shows a schematic representation that illustrates the applicability of the proposed PDC.

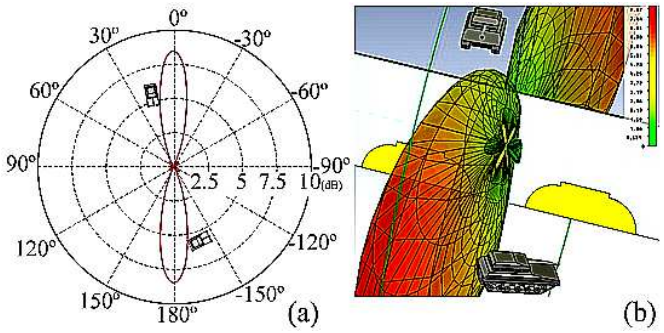

Fig. 1. Radiation diagram of the UWB transmitter, created using a PDC array to illustrate a possible application. (a) Polar Fairfield, and (b) 3D Fairfield obtained with adjustment parameter PDC =0000_B, 0000_B, 0000_B, and 0000_B.

This paper is organized as follows: Section II presents the PDC circuit architecture and design; Section III presents the antenna used in Electromagnetic (EM) simulations, Sections IV and V present the Spice and EM simulation results, while Section VI presents the conclusions.

II. MODELING AND DESIGN

All circuit and layout design of the proposed PDC were designed through the techniques of VLSI full custom using a Spice simulation environment and integrated with the LTSpice 4 and MicroWind 3 design tools. The design rules were those provided by IBM (7WL_4LM_ML_HK) foundry processes in 0.18um SiGe technology. For schematic and post-layout simulations, we considered effects of vertical and horizontal crosstalk coupling input noise variation with 10% of Vdd amplitude, and parameters processes variation by Monte Carlo.

According to Rabaey, Chandrakasan and Nikolic [9], it is possible to model the basic delay element as a first-order RC network, shown in Figure 2. The delay that the transient experiences in this RC network can be observed when applying a transition from logic low-to-high (Vin from 0 to Vdd). The transient response behavior of this circuit is exponential, given by equation (1) [9],

$$v_{out}(t) = \left(1 - e^{-t/RC}\right) \quad (1)$$

where ***R*** is the resistance and ***C*** is the capacitance of the output node, both of delay element.

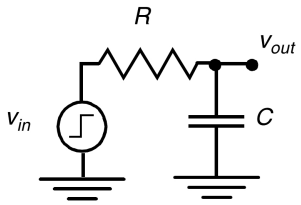

Fig. 2. First order **RC** network [9].

Another basic element of delay is the static inverter, which is the heart of all digital projects and its symbol is illustrated in Figure 3 (a).

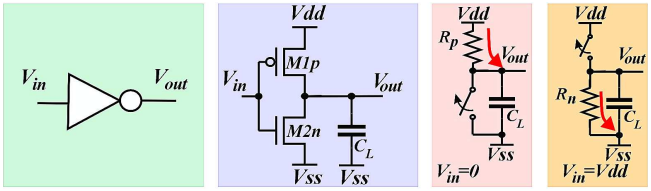

Fig. 3. Static Inverter: (a) its symbol, (b) electrical schematic with two complementary transistors and the capacitance of the output node (C_L) and key model of the dynamic behavior of the static inverter $\mathbf{V_{in}}$=0 in (c),and $\mathbf{V_{in}}$=**Vdd** in (d) [9].

According to Rabaey, Chandrakasan and Nikolic [9], the static inverter consists basically of two CMOS transistors (Fig. 3(b)), being a PMOS (M1p) and a NMOS (M2n), and the capacitance of the output node ($\boldsymbol{C_L}$), which is composed of the transistor drain capacitance, by the capacitance of the metal via and by *fan-out* capacitance. This model can be studied with the aid of key model, being the CMOS transistor considered an open key (infinite resistance) for $|v_{gs}|<|v_t|$ and closed key (finite resistance) for $|v_{gs}|>|v_t|$.

Neglecting the transition time of the input voltage ($\boldsymbol{V_{in}}$), i.e., considering an instantaneous transition from low-to-high logic level, from now on represented as 1→0 (Fig. 3 (c)), there is a transition time of 0→1 in $\boldsymbol{V_{out}}$ which will be determined by the charging time of the capacitor $\boldsymbol{C_L}$ through the channel resistance of the transistor M1p (R_p). The opposite also applies (Fig. 3 (d)), when there is a transition in the input voltage $\boldsymbol{V_{in}}$ of 0→1, with the transition time of the output voltage $\boldsymbol{V_{out}}$ of 1→0 determined by the relation $\boldsymbol{R_n}$ and $\boldsymbol{C_L}$.

Therefore, it is possible specify that the delay time ($\boldsymbol{t_p}$) of the signal is directly proportional to capacitance $\boldsymbol{C_L}$ and the resistance $\boldsymbol{R_{(n\ or\ p)}}$, which, according to Rabaey, Chandrakasan and Nikolic [9], can be represented by the equation,

$$t_p = \ln(2)\, C_L \left(\frac{R_n + R_p}{2}\right) \quad (2)$$

In the dynamic model, R_n and R_p are considered respectively as the resistances of the transistors NMOS and PMOS during the time of interest. Therefore, a basic adjustable delay element can be obtained with the static inverter with adjustment control, the channel transistors resistance (Fig. 4(a)), of capacitances (Fig. 4(b)), or both (Fig. 4(c)).

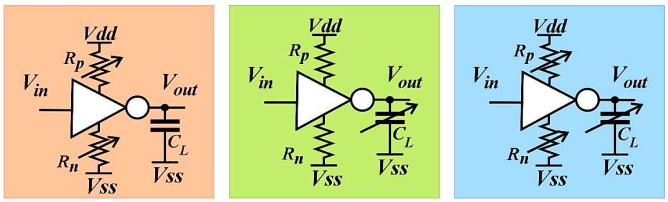

Fig. 4. Diagram of a basic delay element formed by the static inverter. (a) Time adjustment for the change in resistance, (b) of capacitance and (c) both.

A drawback of using the inverter as a basic delay element is the fact that it reverses the signal. Therefore, although there is a real delay in signal propagation, it suffers logic level inversion, which is not always interesting. In order to solve this problem, an arrangement with two inverters, connected in series, can be used. However, in this case, in addition to the load capacitance ($\boldsymbol{C_L}$), it should be taken into consideration the gate capacitance ($\boldsymbol{C_g}$) of input of the inverter output, which will directly influence the propagation time of the signal. Here, both are proportional to the size of the transistors gates, thus, Rabaey, Chandrakasan e Nikolic [9] defined,

$$C_{int} = \gamma C_g \quad (3)$$

where $\boldsymbol{C_{int}}$ is the intrinsic capacitance of the inverter output and $\boldsymbol{\gamma}$ is the factor of proportionality associated with the process technology and usually is close to 1 in most technologies [9].

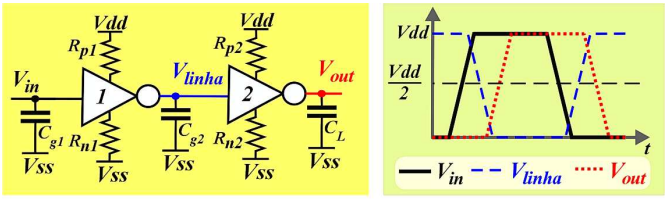

Fig. 5. Delay element formed by two inverters static (a) and its respective waveforms illustrates (b).

In the case where two identical static inverters are associated (Fig. 5(a)) to create a delay element, the problem of signal inversion can be solved. However, it should be considered other features that influence the $\boldsymbol{t_p}$. In this case, it is considered that the $\boldsymbol{t_p}$ will be directly proportional to the intrinsic time delay of the inverters ($\boldsymbol{t_0}$) and according Rabaey, Chandrakasan and Nikolic [9], it is given by the equation (4),

$$t_p = \ln(2)\, C_L \left(\frac{R_n + R_p}{2}\right)\left(2 + \frac{{C_{g2}}^2 + C_{g1}C_L}{C_{g1}C_{g2}}\right) \quad (4)$$

which indicates that the propagation time is larger than twice the propagation time of a basic element formed with a static inverter. Once, in addition to considering the isolated capacitances of each inverter, one should also consider the gate capacitance, in addition to the metal via capacitance between the two inverters. The result of the delay in this topology is shown in figure 5(b), where the transition $\boldsymbol{V_{linha}}$ occurs after the transition $\boldsymbol{V_{in}}$ and before transition $\boldsymbol{V_{out}}$, being that $\boldsymbol{V_{out}}$ now is not inverted as a function of $\boldsymbol{V_{in}}$.

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Once it is obtained a basic delay element that does not invert the output signal as a function of its input, a variable delay element can be built, by varying any of its resistive or capacitive characteristics, or both.

Figure 6(a) illustrates the basic topology of the delay element formed by two static inverters connected to each other via an internal line with a capacitance with ***Vss*** that can be varied to provide different delay times. This capacitance directly influences the rise and fall times in tension V_{linha}. Once chosen the electrical characteristic that is used to control the delay, now it is necessary to choose the type of variable capacitor.

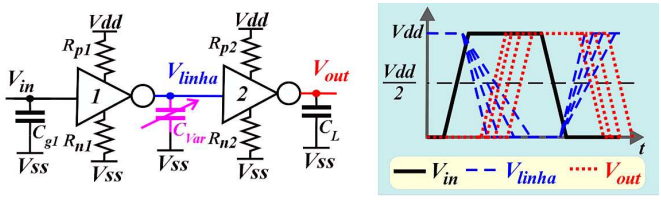

Fig. 6. Variable delay element formed by two static inverters (a) and its respective illustrated waveforms (b).

Here we propose the use of a digitally controlled capacitor with 4 control bits to integrate the programmable controller delay, as shown in Figure 7(a). The detail of the discretely adjustable capacitor is illustrated in Figure 7(b), where all four NMOS transistors have a channel width (***W***) equal to 0.7µm and length (***L***) of 0.18µm and capacitors are all multiples of 1,5fF. Figure 7(c) shows the symbol of the proposed PDC.

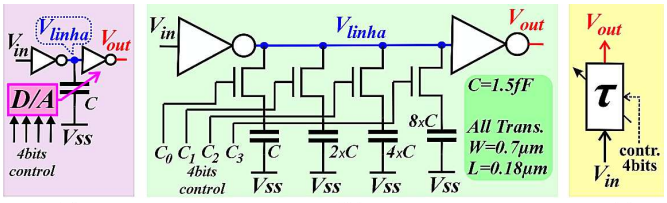

Fig. 7. (a) a programmable controller delay of 4 bits, (b) schematic detail of the variable capacitor and (c) symbol of proposed PDC (DE OLIVEIRA, *et al.*, 2012).

Figure 8 shows the layout of proposed PDC without the pads, where it is shown 4 bits control (C1, C2, C3, and C4) and V_{in} inputs, and V_{out} output of circuit. Guard rings are used for minimize latch-up effects. The circuit occupies an area of 7µm x 16µm.

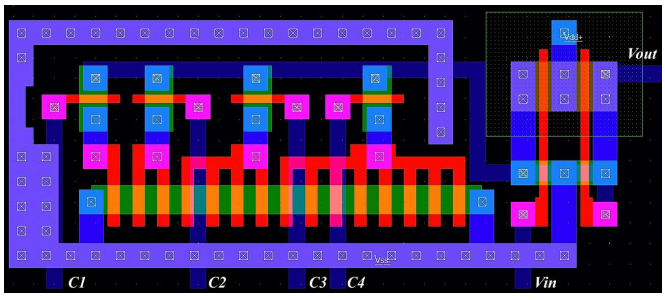

Fig. **8**. Layout of the one channel of the proposed PDC.

III. The Antenna Array Used in Simulations

In order to demonstrate the application of PDC, an array of four antennas of Patch type was prepared, as shown in Fig. 9. With this arrangement, it was possible to collimate the beam to an angular opening of 26 degrees (3 dB) with 8.5dB directivity and sidelobe-12.2 dB, as shown in the elevation radiation diagram of Figure 1.

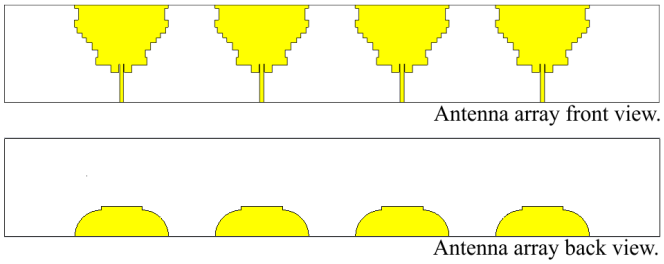

Fig. 9. Front and Back size view of proposed antenna array for the tests.

This array is formed by four identical antennas, illustrated in Fig. 10, which were firstly used by De Oliveira *et al.* [10], in UWB radar application.

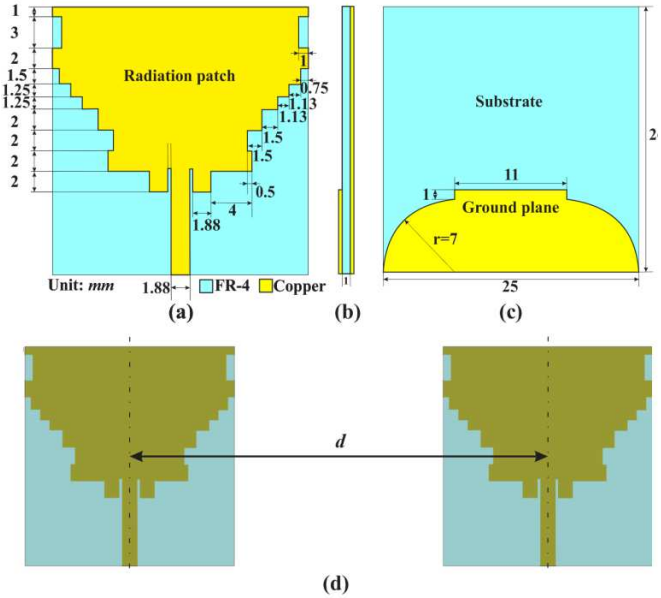

Fig. 10. Geometry of the antenna. (a) Front view. (b) Side view. (c) Back view. (d) Distance between the four antennas of the array [10].

The antenna, which has a total volume of 25 x 26 x 1 mm³ and total antenna array volume of 175 x 26 x 1 mm³, is printed on both the front (radiating element microstrip feed line) and the back (the ground plane) faces of a FR-4 substrate 1mm thick and with dielectric constant of 4.3 [10].

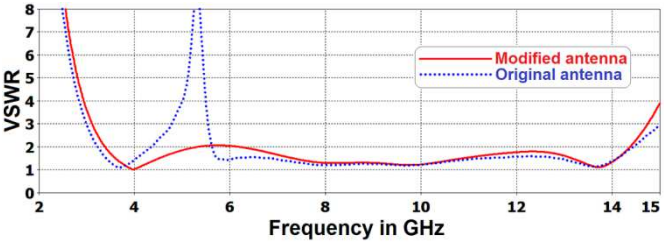

Fig. 11. Simulated VSWR with adopted antenna in solid line and original antenna in dotted line [10].

The U-shape, proposed by [4] in the original antenna, was removed by De Oliveira *et al.* [10] because it favored the response between 3.7 and 4.3GHz. Fig. 11 compares the Voltage Standing Wave Ratio (VSWR) plots for both antennas.

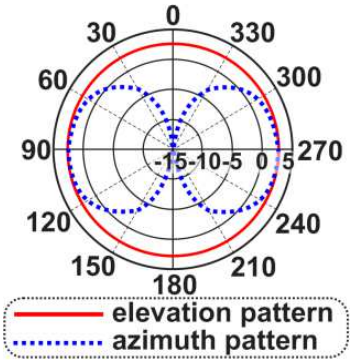

Fig. 12. Simulated radiation patterns at 4GHz with elevation in solid line and azimuth pattern represented in dotted line [10].

The single antenna radiation pattern is shown in the radiation pattern of Fig. 12.

IV. PDC SPICE SIMULATIONS RESULTS

The simulation of PDC circuit in post-layout Spice model shows a controlled delay between 0 and 97.4 ps. Figure 13 shows some possibilities for delay for digital control words 0000_B, 0001_B, 1000_B, and 1111_B. The dark-solid line shows the results for an input pulse ***Vin*** with 2 V of amplitude and 487 ps of width. The dash-doted blue lines represent the internal PDC signal (V_{linha}) for the four different control words in sequence, while the doted red lines represent the output signals of PDC with a delay for each control word.

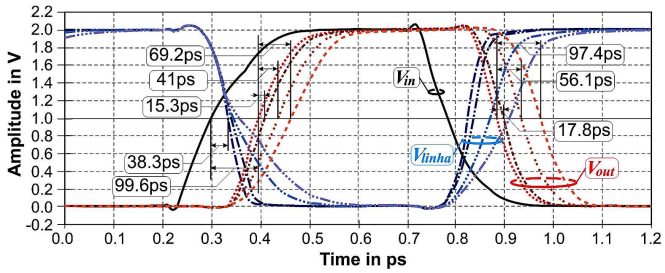

Fig. 13. Waveforms of the transition (low-to-high and high-to-low) of PDC for different settings.

In the first case, with the control word 0000_B, the intrinsic delay of the circuit is 99.6 ps. Since the proposed PDC was designed to work together for at least two PDCs, this intrinsic delay will be disregarded, which leads to the condition without delay. In the next cases, with the control word 0001_B, it is observed a delay of 15.3ps for rise time, and of 17.8ps for fall time. For control word 1000_B, they are respectively 41ps and 56.1ps, and finally for the control word 1111_B, they are respectively 69.2 and 97.4ps.

Regarding the radar application for the proposed circuit, in order to allow the beamforming in technology Timed-Array with UWB (pulses with a frequency range of GHz), it is required that a precise control of the delay between signal of each antenna of the array reach the range of picoseconds. Here we present the architecture adopted for the precise delay control.

Figure 14(a) shows the proposed PDC in array topology (PDC array) [8]. The circuit consists of four independent channels, with details shown in Fig. 14(b). Each channel consists of a delay line formed basically by two inverters, and between both inverters (at ***line***$_i$ node) a digital variable capacitor is introduced, which consists of four capacitors with one node at V_{ss} and the other terminal at a nMOS switch controlled by signals C0-C3 (the other terminal of the switches is connected at node ***line***$_i$).

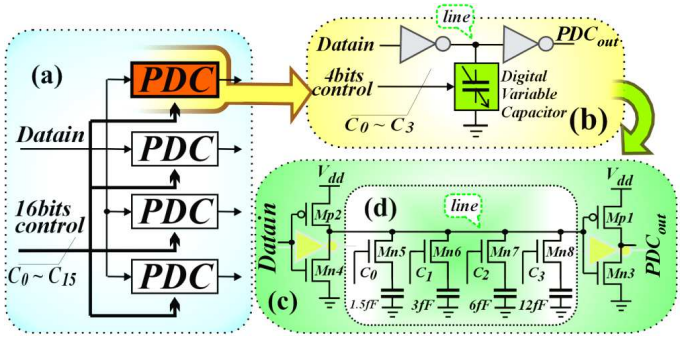

Fig. 14. General PDC array: (a) PDC array; (b) PDC Unit; (c) PDC schematic; and (d) Digital variable capacitor.

The instant when a transition occurs from low-to-high at the input of the first inverter, its output begins a transition from high-to-low of line node signal. However, this transition time varies depending on the configuration of the variable capacitor which will attach one, two, three or four capacitors. Additionally, to increase the delay more effectively, the four capacitors are not with a same value, but start at 1.5 fF (controlled by C0) and doubles the value for the its adjacent one, thus becoming 1.5fF, 3fF, 6fF and 12fF, respectively. The high-low transition leads to a low-high transition in the second inverter output, signal ***PDC***$_{out\_i}$, and the delay values depend similarly on the capacitive load controlled by C0-C3. Furthermore, the same is true for low-high transitions of the first inverter, but this is not critical, since only the high-low transition matters for the UWB pulse generation.

V. PDC EM SIMULATIONS RESULTS AT UWB TIMED ARRAY RADAR APPLICATION

In order to demonstrate the applicability of UWB Radar in PDC, we designed a transmitter beamforming four identical channels, each one consisting of a PDC in series with a UWB pulse generator and an antenna. The UWB pulse generator used to obtain the UWB pulse, during the post-layout SPICE simulations, was recently proposed by De Oliveira *et al.* [10]. The architecture of the transmitter beamforming (by timed-array capability) is shown in Figure 15.

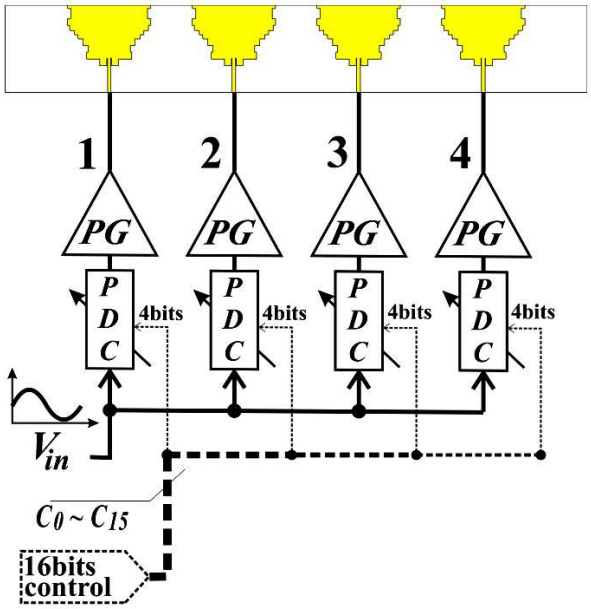

Fig. 15. A general structure of beamforming transmitter used in simulation tests.

Electromagnetic simulations (EM) were performed in CST Microwave Studio 2011. Initially, the PDCs were adjusted with parameters (1111_B, 1000_B, 0010_B, and 0000_B) which generated the following delays: 96ps on channel 1; 45ps on channel 2; and 18ps on channel 3. The channel 4 did not delay the stimulus signal. As a result of this configuration, we obtained a beam directed to the tank ahead as shown in the diagram irradiation in polar form (Fig. 16(a)) and the 3-D shape (Fig. 16(b) at central frequency of 4GHz.

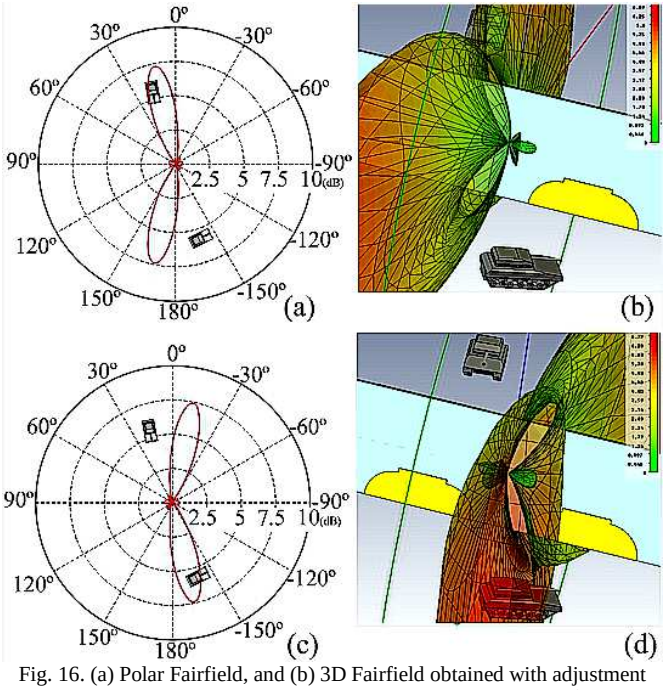

Fig. 16. (a) Polar Fairfield, and (b) 3D Fairfield obtained with adjustment parameter PDC =1111_B, 1000_B, 0010_B, and 0000_B. (c) Polar Fairfield, and (d) 3D Fairfield obtained with adjustment parameter PDC = 0000_B, 0010_B, 1000_B, and 1111_B.

Then, the PDCs were adjusted with opposite parameters, such as: 0000_B, 0010_B, 1000_B, and 1111_B. As a result, there was a beam directed toward the behind of the tank, as shown in the diagram irradiation in polar form (Fig. 16(c)) and the 3-D shape (Fig. 16(d)).

In the first case, we obtained a beam deflection of approximately 12° with a gain of 7.3 dB and -11dB of sidelode. In the second case, the deflection was 13° with the same gain of 7.3 dB and even sidelobe of -11dB.

VI. CONCLUSIONS

We presented the design of a PDC composed of 0.18 µm SiGe CMOS technology through an integrated Spice environment with MicroWind 3 and LTSpice 4 VLSI Full custom project tools. The Spice simulation results showed a controllable delay time between 0 and 96ps, which, in the EM tests, with CST Microwave Studio 2011, resulted in a controlled beam with center frequency of 4GHz, with angular width of 27° and variable deflection between 12º and -13º, with a 8.3dB directivity and sidelobe of -11dB. This control was achieved using a digital variable capacitor between the transition line of two static inverters and the ground line that allows controlling of time charging and discharging of the variable capacitor and consequently, control of delay times.

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