Design and Analysis of a two-Stages Miller Compensated OpAmp for High-Speed applications

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***Abstract* — Defense Applications need high-performance systems. In the last few years, Brazilian Air Force has bought several new aircrafts, which are equipped with the most developed Electronic Warfare avionics. But all of these equipments are bought from foreign companies, letting BAF exposed to a probable embargo. In this context, it is highly desirable to develop our own avionics, which must be necessarily based on a SoC design and on ICs platforms. Operational Amplifiers (OpAmps) serve as the basic building blocks in almost every analog and mixed-signal electronic circuit. Especially when focusing on complex circuits, they must be fully designed from the beginning, achieving improved performances. In this paper it is presented the design of a Two-stage Miller Compensated OpAmp for high-speed Applications. The circuit is designed in the 0.35µm CMOS technology, process C35B4C3 of AustriaMicroSystems. LTSPICE software was used for simulation and results show that the OpAmp has a 88.6dB open-loop DC gain, a unity gain-bandwidth of 120.7 MHz, a Phase Margin of 60.3º and a Slew rate of 76.2V/µs, when driving a load of 1pF. It shows an improved performance when compared to previous ones found in literature, presenting a high slew rate and a high DC gain simultaneously. The device performance was verified positively both at the schematic and at the layout level, showing a high potential to practical implementations.**

Keywords— Operational amplifiers; Analog integrated circuits; Analog Design.

I. INTRODUCTION

Defence Applications need high-performance systems. In the last few years, Brazilian Air Force has bought several new aircrafts, which are equipped with the most developed Electronic Warfare avionics. But all of these equipment are bought from foreign companies, letting BAF exposed to a probable embargo. In this context, it is highly desirable to develop our own avionics, which must be necessarily based o a System on Chip (SoC) design and on Integrated Circuits (ICs) platforms. These circuits must support high-speed applications, while providing accurate and reliable results.

Operational amplifiers are the basic cell in almost every analog integrated electronic circuit. They require a proper design according to the functionalities and specifications of each project. Contemporary systems, especially the mixed ones, increasingly need components that work fast enough to deal with high frequency signals, leading to fast-response circuits. This challenge increases even further as the voltage supply and transistors channel lengths shrink. It shows to be a common trend, since a lower power consumption and portability are desirable features in most modern electronic devices.

The main bottleneck in designing a high-speed OpAmp is the existing tradeoff between speed and gain. A high DC gain component demands multistage design, long-channel transistors an low bias current, whereas a high speed one demands single stage design, short-channel devices and high bias current levels [1,2]. In this context, in order to accomplish very-high performance projects, it is necessary to find a trade-off between these quantities, generally using some kind of optimization process.

This paper presents an OpAmp design that covers both a high slew rate and a high DC gain simultaneously. Moreover, the use of Miller compensation ensures the combination of a high gain bandwidth and a high phase margin, sustaining the stability of the amplifier even in high-frequency operation. Therefore, it achieves a high speed performance whilst maintaining the other parameters at a competitive level when compared to previous works using similar technology. As an example, a DC gain of 77.3dB, with GBW of 14.1MHz and a slew rate of 10V/µs was achieved in [3] for a 0.35µm CMOS technology, but using 5V operating voltage. Using the same technology, a DC gain of 55dB and 12.5V/µs was achieved in [4], but with a 6V operating voltage. On the other hand, the OTA in [5] achieves a DC gain of 93.27dB, with 9.32MHz GBW and a slew rate of 36V/µs, also with a 5V supply. These background works evidence the aforementioned competitive level of our work and its high potential to be practically implemented.

II. TWO STAGE OPAMP DESIGN

The proposed design is based on basic OpAmp equations and topology already presented in [6], followed by optimization processes focusing on increased slew rate and gain bandwidth. This improved process has been obtained by computer simulations using the software LTSpice (the same used internally by the developer company, Linear Technology [7]), and using 0.35µm CMOS technology libraries of AustriaMicroSystems.

The topology is a two stage OpAmp, as shown in Fig.1, where the first one is a differential gain stage. A compensation structure has been placed so as to enhance the system frequency response. The topology is well known, however an optimization process of the parameters made its performance to be above average.

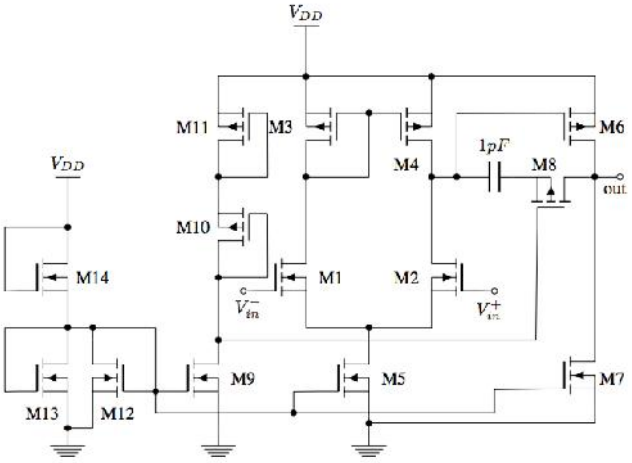

Fig. 1. Schematics of the Operational Amplifier design topology.

A. Description of the circuit

In Fig.1, transistors M1 and M2 form a differential input pair, driving the current mirror formed by M3 and M4, as a load, and being biased by the current sink formed by M5. The output is controlled by the differential voltage between V_{in}^- and V_{in}^+. If $V_{in}^- > V_{in}^+$, the output is ideally 0, whereas if the opposite occurs, the output is ideally V_{DD}. In practice, there is a transition that is not so abrupt.

It is necessary a second gain stage so as to increase the gain and make the transition faster, i.e., to create a high gain region. Transistor M6 operates in the standard common source configuration and, thereby, amplifies the output signal from the first stage, being biased by the current sink formed by M7.

Transistor M12 forms a current mirror with M5, M7 and M9. The sub-circuit input current is defined by the bias voltage in M12 drain, which can be defined by the voltage divider composed by M13 and M14.

The main idea of Miller compensation is to change the position of the poles so as to improve stability, i.e., the Phase Margin. Firstly, a compensation capacitor C is used, creating a feed-forward path through it. This procedure, however, generates a zero in the system transfer function that limits the unity gain frequency. Since a high bandwidth is desired, a way to control this zero is adding a nulling resistor R_c in series with such capacitor. However, resistors tend to have big dimensions in integrated circuits. Thereby a transistor operating in the active region, and thus simulating a resistor, is the best option. That is the function of M8. Transistors M11, M10 and M9 are also included in order to bias M8, whose resistance depends on the gate-source bias voltage.

B. Design Procedure

A preliminary project was performed using the procedure described in [6], which is shown here by equations (1) to (15), considering the technology parameters. Equations will be presented chronologically in this paper, depending on their influence to the project.

It is also necessary to define the specifications of the OpAmp so as to have a first approach. As aforementioned, the most relevant features for this design should be high open-loop gain, slew rate and gain bandwidth, simultaneously. They can be seen in Table I. Two additional parameters are added to specifications once they are important for the design procedure – the maximum and minimum input voltage level. The larger the input voltage range, better is the OpAmp. Nonetheless, it has been converted into another degree of freedom of the project, as long as the design inequations are satisfied.

Table I: Specifications for the OpAmp

Parameter	Value
Open-loop Gain	90dB
Slew Rate	50 V/µs
Gain Bandwidth	100 MHz
Phase Margin	60º
Vin (min)	0.9 V
Vin (max)	2.8V

$$C_c > 0.22C_L \tag{1}$$

$$I_5 = SR.C_c \tag{2}$$

$$S_4 = S_3 = \frac{2I_3}{K_p[V_{DD} - V_{in(max)} - |V_{T3}| + V_{T1}]^2} \geq 1 \tag{3}$$

$$\frac{g_{m3}}{2C_{gs3}} > 10GB \tag{4}$$

$$g_{m2} = g_{m1} = GB.C_c \implies S_1 = S_2 = \frac{(GB.C_c)^2}{K_n I_5} \tag{5}$$

$$V_{DS5(sat)} = V_{in(min)} - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1} \geq 100mV \quad (6)$$

$$S_5 = \frac{2I_5}{K_n[V_{DS5(sat)}]^2} \quad (7)$$

Equations 1 to 7 are responsible for the performance of the input stage. Slew Rate and Gain Bandwidth (GBW) are roughly defined by them and, also, the first stage open loop gain. The smaller the compensation capacitance is, the higher the slew rate is and also the dominant pole. However, a high capacitance is required for driving low impedance loads, leading to a trade-off. Increasing the width of input transistors would be a way to increase GBW, but it does not show to be very efficient, once the circuit dimensions increase a lot.

$$g_{m6} = 10g_{m1} \quad (8)$$

$$S_6 = S_4\frac{g_{m6}}{g_{m4}} \quad (9)$$

$$I_6 = \frac{g_{m6}^2}{2K_pS_6} \quad (10)$$

$$S_7 = S_5\frac{I_6}{I_5} \quad (11)$$

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)(\lambda_6 + \lambda_7)} \quad (12)$$

Equations 8 to 12 are responsible for the output stage, considering the second stage open-loop gain and, thus, the overall gain. Higher values of M6 width lead to higher gains, but implying in bigger circuits. It is also worth to mention the importance of the parameter I_5, drain current of transistor M5, which is responsible for the gain of the circuit.

$$S_{11} = S_6\frac{I_{11}}{I_6} \quad (13)$$

$$S_9 = S_5\frac{I_{11}}{I_5} \quad (14)$$

$$S_8 = \frac{C_c}{C_L + C_c}\sqrt{\frac{S_{10}S_6I_6}{I_{11}}} \quad (15)$$

Equations 13 to 15 are responsible for the Miller compensation sub-circuit. Transistors dimensions are designed so that M8 may implement the aforementioned nulling resistor R_C.

$$\frac{S_{12} + S_{13}}{S_{14}} = \frac{K_nS_5\left(V_{DD} - 2V_T - \sqrt{\frac{2I_5}{K_nS_5}}\right)^2}{2I_5} \quad (16)$$

Equation 16 relates M12, M13 and M14 dimensions, so as to bias the current sinks (M5 and M7).

Following this setup, the values of the transistors were assessed and are displayed in Table II, considering the compensation capacitor as 1pF and all the transistors lengths as 1µm.

Table II: Preliminary dimensions of transistors

Transistor	W/L
M1 and M2	41.7
M3, M4 and M11	11.7
M5	4.2
M6	510
M7	91.9
M8	74.7
M9 and M12	5
M10 and M14	1
M13	27

Using the dimensions of table II, the two-stage OpAmp was simulated using 0.35µm AMS (AustriaMicroSystems) CMOS libraries, in LTSpice Simulation.

A subsequent optimization has been made so as to achieve the project specifications, by adjusting the biasing circuit to provide I_5 as specified (varying M13 width), and the Miller compensation system to provide the Unity Gain Frequency (by varying M8 width). The new values for M13 and M8 widths were both 11µm. After running the simulation, the results were as shown in table III.

Table III: Preliminary Results of the circuit

Parameter	Value
Open-loop Gain	85.7dB
Phase Margin	85º
Unit Gain Frequency	100 MHz
SR+	44 V/µs
SR-	44 V/µs
Supply Voltage	3.3 V
Load Capacitor	1 pF

A second optimization process was held, this time focusing on the reduction of the size of the transistors, keeping the general performance of the amplifier. Firstly, M6 width was reduced and M7 was adjusted to the highest value of open loop gain. Secondly, the pair M3 and M4 was adjusted with M5 to achieve a large gain bandwidth and, thus, compensate the reduction in M6 width.

The third and last optimization process aims a new enhancement of the performance of the OpAmp, finding out possible tradeoffs so as to achieve better results. The main performance parameters (gain bandwidth, slew rate and open loop gain) are functions of the drain current of M5, I_5, but behave in opposite ways. The chosen parameter was the M13 width.

Figures 2 and 3 show the trade-offs between outputs that are being optimized: slew rate, open loop gain and gain bandwidth. So as to make a decision, a phase margin of 60º, which the usual minimum projected value, was used as the optimal point.

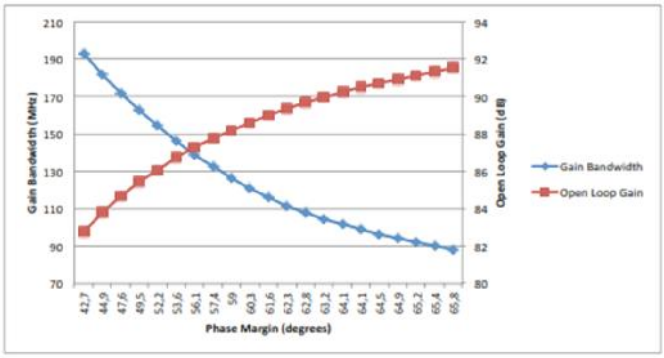

Fig. 2. Trade-off between open-loop gain and Gain Bandwidth varying M13 width from 5 to 25µm..

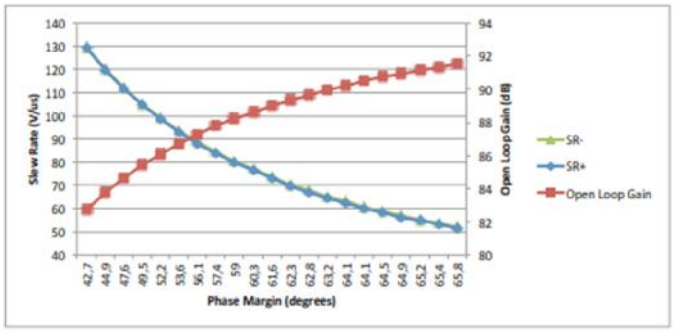

Fig. 3. Trade-off between Slew Rate and Open Loop Gain varying M13 width from 5 to 25µm.

Therefore, after all the optimization processes, the final values for the dimensions of the transistors were set and are presented in table IV.

Table IV: Final dimensions of transistors

Transistor	W/L
M1, M2 and M7	30
M3, M4 and M11	38.5
M5	10
M6	215
M8	7
M9 and M12	5
M10 and M14	1
M13	14

With these dimensions, the simulation was run once again and, for a 1pF load the performance was as described in Table V. Figures 4 and 5 show transient and AC analyses, respectively.

Table V: Preliminary Results of the circuit

Parameter	Value
Open-loop Gain	88.6 dB
Phase Margin	60.3º
Unit Gain Frequency	120.7 MHz
SR+	76.2 V/µs
SR-	77.1 V/µs
Supply Voltage	3.3 V
Load Capacitor	1 pF

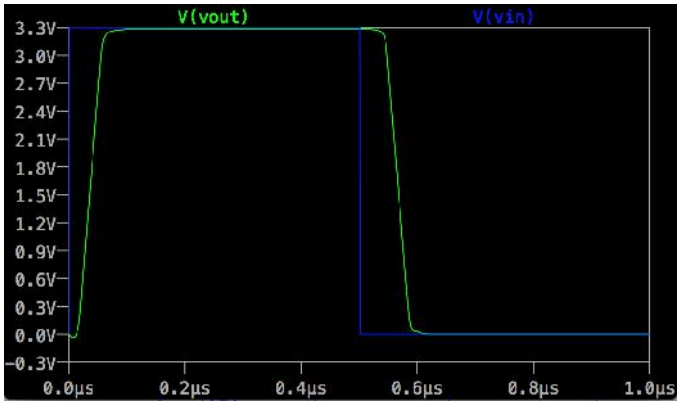

Fig. 4. Transient analysis considering the final dimensions.

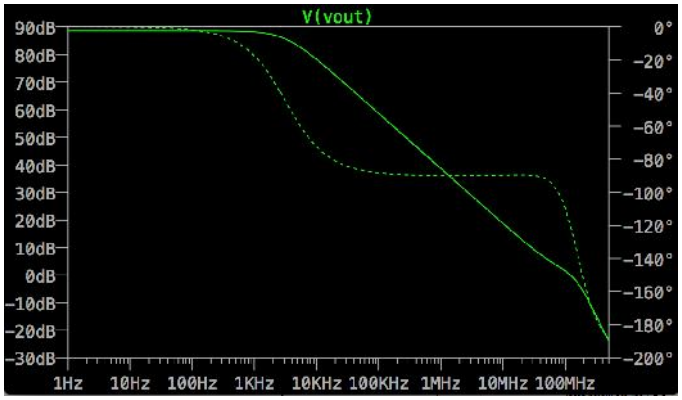

Fig. 5. AC analysis considering the final dimensions.

III. LAYOUT DESIGN AND CONSIDERATIONS

The layout design is an important step in designing a VLSI circuit. The first essential point is that a proper layout may reduce manufacture variations, for example, in mismatched transistor pairs. The second one is that it must be directed to the reduction of the total area, thereby reducing production costs. Nevertheless, all this procedure must be done considering eventual parasitic capacitances due to metallization.

It is of main importance that the input differential pair of the OpAmp (M1 and M2) is built with matched transistors. Process variations may lead to a substantial decrease in the system gain, which is not desirable. So there are some strategies to reduce this interference.

The approach that has been used in this design is the interdigitized layout, once it averages the process variations among the parallel transistors. The same approach has been used for the current mirror (transistors M3 and M4), that work as the load of the input pair. In order to have the OpAmp working, they are designed to have the same dimensions. In this case they are displayed in a vertical arrangement to ease their gates connections, sharing the same gate, and also reducing the total circuit area.

At first, it can be noticed two large components, which are the 1pF capacitor (50µm *x* 50µm) and the 215µm transistor (M6). So as to reduce the area covered by the circuit it is fundamental to work on these two items, since the initial expected area would be over 50µm *x* 215µm ≈ 0.01mm^2.

Since W >> L, the strategy that was used is to associate "*n*" transistors with a width "*1/n*" of the original width. In this case, it was chosen n = 10, which would make the transistor width correspond to almost half the capacitor one. A similar approach, with a different value of *n*, was applied to other transistors, with relative high width (M1, M2, M3, M4, M7 and M11). In the cases of M1, M2, M3 and M4, this strategy had already been used, but with matching purpose.

Metallization usually contributes to increase the parasitic capacitances and resistances in the design. On the other hand, extremely narrow lines may lead to high resistance.

One way to reduce metal is to simply make the components closer. Due to process limitations, it is not possible to place to transistors in a distance less than 2λ from each other, but it is possible to make many transistors in the same N-well region sharing their common nodes and therefore no extra metal connection is needed. This strategy was used to project the bottom transistors (M5, M9, M12 and M13).

Also, it can be noticed that it had already been used with the matched pairs transistors, so there are actually two advantages of this approach. After all these considerations, the final layout is the one found in Fig.6. The final layout area is 0.004mm^2 , which shows a reduction of 60% when compared to the first proposed layout, without applying layout techniques and considerations.

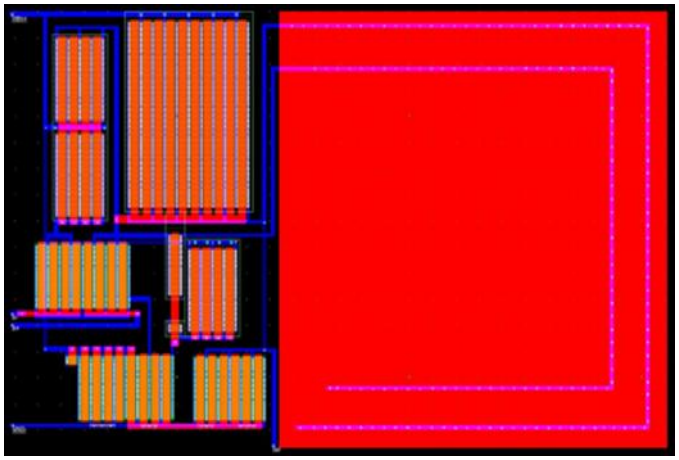

Fig.6. OpAmp final layout, considering described techniques and considerations.

IV. DISCUSSION

After re-simulating the project, it is easy to conclude that it presents high slew rate and gain bandwidth, when compared to the aforementioned references found in literature (i.e., [3], [4] and [5]) and also keep the open loop gain at a competitive level, as it is shown in Table VI. Besides attending the initial specifications, it is worth to point out that this design achieves all specifications with a low voltage supply, which is

important for reducing power consumption; and with a reduced area, which is fundamental for circuit integration.

Table VI: Results Comparison

Parameter	Our design	Ref.[3]	Ref.[4]	Ref.[5]
Open-loop Gain	88.6	77.25	55	93.27
Phase Margin	60.3	85.85	110	93.14
GBW (MHz)	120.7	14.1	Not mentioned	9.32
Slew Rate (V/µs)	76.2	10	12.5	36
VDD-VSS (V)	3.3	5	6	5
Load Capacitor (pF)	1	10	5	5
Area (mm^2)	0.004	0.01 (estimation)	0.01 (estimation)	0.089
C_C (pF)	1	3	5.5	Not used

Finally, so as to make a better comparison, Fig.7 shows the variation of the OpAmp performance when the load capacitance increases. The open loop gain and the low-to-high slew rate do not change, but the gain bandwidth and the high-to-low slew rate do. Nonetheless, the system still works with a higher slew rate and GBW compared to the used references.

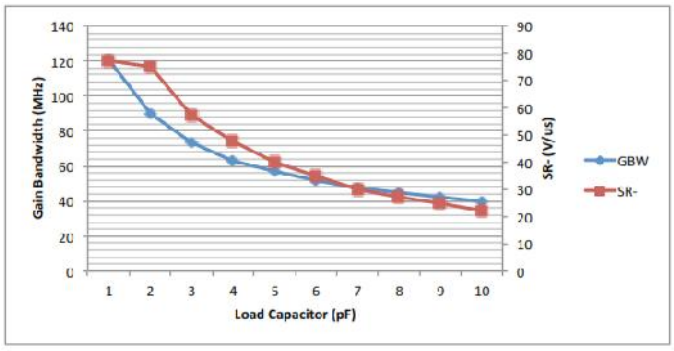

Fig.7. Performance variation according to the load capacitance.

V. CONCLUSION

The design of a Two-stage Miller Compensated OpAmp for high-speed Applications was presented, including the specifications, preliminary design and further optimizations.

The circuit was designed in the 0.35µm CMOS technology. LTSPICE software was used for all simulations, showing an 88.6dB open-loop DC gain, a unity gain-bandwidth of 120.7 MHz, a Phase Margin of 60.3º and a Slew rate of 76.2V/µs, when driving a load of 1pF. The device performance was verified positively both at the schematic and at the layout level. Layout techniques were implemented in order to reduce area, capacitances and resistances.

The final design and layout show a very good performance when compared to previous works found in literature, presenting a high slew rate and a high DC gain simultaneously, and showing a high potential to practical implementations.

REFERENCES

[1] Kush Gulati and Hae-Seung Lee, A High-Swing CMOS Telescopic Operational Amplifier, IEEE Journal of Solid-State Circuits, Vol. 33, No.12, pp 2010-2014, December 1998.

[2] D.S. Shylu, D.J. Moni and B. Kooran, Design and Analysis of a Two Stage Miller Compensated OP-AMP Suitable For ADC Applications, International Journal of Research in Engineering and Technology, Vol.3, No.7, May 2014.

[3] Amana Yadav, Design of Two-Stage CMOS Op-Amp and Analyze the Effect of Scaling, International Journal of Engineering Research and Applications (IJERA), Vol.2, Issue 5, September-October 2012, p.647654

[4] Kumar Saurabh and P. Raja, Comparative Study on CMOS Based Operational Amplifier, International Journal of Technical Research (IJTR) Vol.2, Issue 2, Jul.-Aug. 2013.

[5] Nordiana Mukahar, Siti Hawa Ruslan and Warsuzarina Mat Jubadi, Operational Transconductance Amplifier Design for A 16-bit Pipelined ADC, 2nd Engineering Conference on Sustainable Engineering Infrastructures Development and Management, December 2008.

[6] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 2nd ed. New York: Orford University Press, 2002.

[7] http://www.edn.com/electronics-blogs/anablog/4311849/LTspiceseminar-with-Mike-Engelhardt..