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Emulation-based Validation Procedure for Digital RF Memory Simulator

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***Abstract*— Studies of a digital RF memory (DRFM) operation are necessary to verify its effectiveness in signal reproduction. A good tool for such analysis is a DRFM simulator since it has enough flexibility to vary its parameters. However, to provide reliable results, this simulator must be validated. In this paper, a DRFM simulator is validated through an emulation process using adequate electronic instrumentation. The results were satisfactory since minimal variations were observed when simulated and emulated pulses were compared regarding peak power, sidelobe level, pulse width, bandwidth, frequency, and noise floor.**

***Keywords*— DRFM, Emulation, Simulation, Signal Parameters.**

I. Introduction

DRFM has a relevant function in the electronic jamming process by maintaining the coherence of the emitted signals. However, the technological advance in Electronic Warfare (EW) has improved radars, which can detect the minor differences between the signals generated by the DRFM and its echo radar [1]. Based on this scenario, several studies have sought and still seek to analyze the impacts that certain parameters of a DRFM and its components generate on the reliability of signal reproduction. For example, it was analyzed the effects that a jitter in the sampling time of an analog-to-digital converter (ADC) has on the output of its system [2]. Another researches performs a study on the impacts of changing the number of bits of the DRFM converters on the radar receiver-matched filter [3]. A similar analysis is also made by [4], in which, in addition to this variable, the effects of changing the system sampling rate were studied. Therefore, there is a constant search for increasingly reliable signals. The execution of the aforementioned analyses requires, in most cases, a flexible and adaptive model with a high degree of freedom to cover a large number of variables and parameters. Using a Software Defined Radio (SDR) is one of the existing solutions to circumvent this situation. It happens because an SDR allows the modification of its characteristics quickly and with low financial cost [5]. Motivated by the previously mentioned studies, a DRFM simulator was developed, associated with devices classified as Commercial Off-the-Shelf (COTS). Its main objective is to allow a wide variation in its parameters for analysis and studies. The simulator has a high degree of complexity to the point that its generated signals have high fidelity to those generated by a DRFM in the same configurations.

However, the simple development of a simulator, even if it has been modeled in a complex way and based on its entirety in existing literature, does not bring the reliability and credibility necessary for the results of the simulations. Thus, it is essential to find a way to validate this simulator using real equipment. A possible solution to this problem focuses on combining different hardware, each representing a specific part of the DRFM simulator, to compare the operation of both devices. Thus, an experiment similar to the one proposed by [6] was performed in which hardware such as a Digital Storage Oscilloscope (DSO) and an Arbitrary Waveform Generator (AWG) were used together, resembling the structure of a real DRFM. Subsequently, the output signals of the emulation process and the simulator were compared in several parameters. The differences between them were minimal, resulting in a simulator validation.

This paper is organized as follows. Section II discusses a theory of DRFM and explains the simulator operation. Section III presents the methodology of the simulations and emulations performed in this work. Section IV discusses the results, ending with Section V, with a brief conclusion.

II. DRFM Simulator

A digital RF memory has great relevance in Electronic Warfare. Because of its wide use in electronic interference [1], we seek to verify the effects on the DRFM output signal generated by the variation of its parameters. To perform the analysis, it was necessary to make an adaptive, low-cost, and versatile model to allow us to make such measurements. Software-defined radio (SDR) covers these requirements even with a low financial value of implementation with COTS. In addition, an SDR allows to perform different system configurations with quick adaptations and updates, enabling them to cover multi-purposes [5].

This paper proposes a DRFM simulator using Matlab software, improving its interface with the Design App software, both from Mathworks. Keeping in focus the main objectives that guided its development, this model allows its user to insert and modify several parameters and variables existing in a DRFM, as seen in the main screen of the simulator shown in Fig. 1. In addition, the operator can use the model in an exclusively simulated environment or associate it with a signal generator and a digitizer with real signals.

For such modeling, selecting one among the several possible architectures of a DRFM was necessary. As this simulator does not aim to serve a single specific digital memory, a basic system architecture was chosen, but one that contained all the common systems belonging to a real DRFM, as proposed in [7]. The block diagram that represents the simulator is shown in Fig 2.

Its operation is based on the mode of operation of a conventional DRFM. A signal injected into the model is initially

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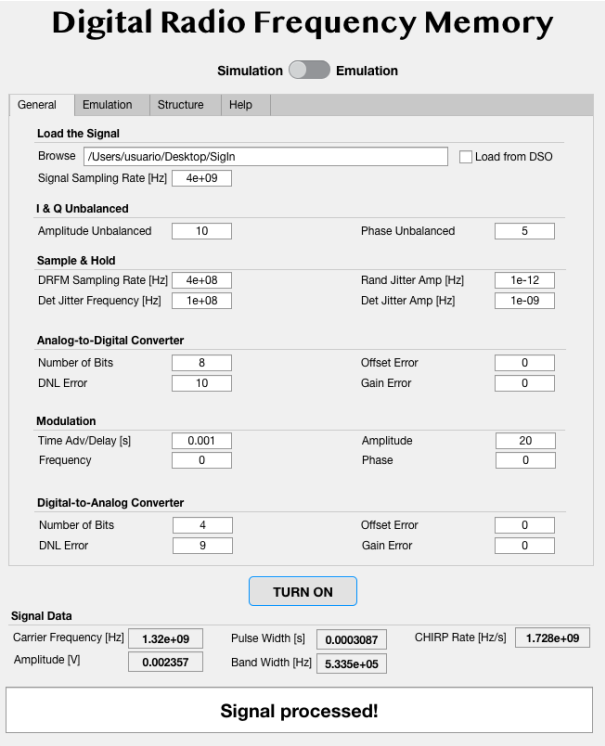

Fig. 1. DRFM simulator interface.

filtered by a bandpass filter using the Kaiser window method. This procedure is necessary since its operation is restricted to signals up to L-band. Sequentially, to perform baseband signal processing as described in [8], an Instantaneous Frequency Measurement (IFM) calculates the frequency of the injected signal and provides this information to the Local Oscillator (LO). The signal is demodulated, resulting in the I (In-Phase) and Q (Quadrature) channels. Finally, the LO generates a signal at the frequency provided by the IFM, and a mixer performs the down-conversion of the signal to the baseband [9].

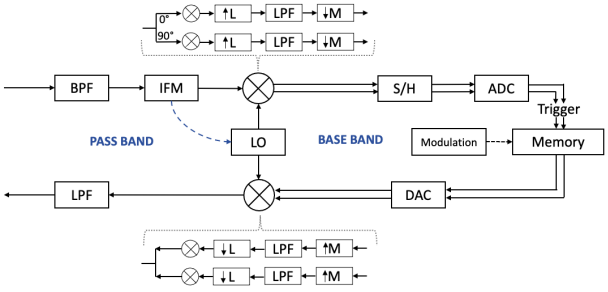

Fig. 2. Modeled DRFM architecture.

However, due to the non-linear behavior of these devices, some unwanted noises and signals can be generated along this process. A specific one is caused by a possible unbalance between the I and Q channels. Theoretically, after the demodulation process, the amplitude of these channels is equal, as well as their phases are offset by exactly 90 degrees. However, a certain difference in their amplitudes and phases is observed in practice. This unbalance has the effect of forming an image in a symmetrical position to the desired signal in the frequency spectrum [9].

Once in the baseband, the signal is submitted to a down-sampling process since there is no need to maintain its high sampling rate. The method described in [10] is used for this purpose in which interpolations and decimations of the signal are performed to acquire the desired sampling rate. To avoid the aliasing effect, the signal must be filtered to remove unwanted spectral components. For this purpose, a low-pass filter with a variable cut-off frequency is used according to the values selected in the simulator.

Subsequently, the signal goes through the digitization process. Obviously, because it is a computational model, it is already discretized. What happens at this stage is the insertion of the errors existing in this process in real equipment. The first deals with small variations in the sampling time performed by the Sample-and-Hold subsystem. This jitter in the time between each operation cycle can have two different behaviors, which are deterministic or random. First, the variation in the time of each cycle follows a specific pattern (sinusoidal, etc.). Its presence is perceived by the appearance of non-harmonic spurious signals lateral to the main signal [3].

In the case of random jitter, the time variation between each cycle is random and does not follow a specific pattern. The effect of its presence is noticed by an increase in the noise floor. Mathematically, its power level can be measured for a special case of a sinusoidal signal as demonstrated by [2]. Taking f as the signal frequency, and σ as the rms (root mean square) value of the jitter, the noise caused by random jitter (N_{Jit}) is given by (in dB)

$$N_{Jit} = 20log(2\pi f\sigma). \quad (1)$$

Other errors that can be simulated are modeled when the signal passes through the ADC. One of them deals with quantization noise. Inherent to all converters of this class, this error is irreversible and generates a signal mischaracterization according to the number of bits and scale of the ADC. One of the effects of its presence is a reduction of the spurious free dynamic range (SFDR) of the system, noticed by the increase of the noise floor. Being q the value referring to a least significant bit (LSB), the power of this noise (N_{Qtz}) is given by [1]

$$N_{Qtz} = 10log(\frac{q^2}{12}). \quad (2)$$

In addition to quantization noise, there are errors related to the converter transfer function. Among the linear errors, gain and offset are two examples that also impact the quality of the digitized signal. Among the nonlinear errors, the Differential Non-linearity (DNL) deals with the maximum size deviation between each LSB of the transfer function [1]. Its effect occurs at the degradation in the signal quality, which can also be modeled mathematically. Since ε is the rms DNL of the ADC and b is its number of bits, the noise power (N_{DNL}) is acquired by [11]

$$N_{DNL} = 20log(\frac{1+\varepsilon}{2^b}). \quad (3)$$

After all this process, the DRFM has a trigger that analyzes the leading edge and falling edge of the pulse. The recording in the DRFM memory only starts when the pulse identification occurs [12]. Once the signal is recorded in the memory,

the simulator operator can perform modulations in phase, frequency, and amplitude of the signal, as well as the insertion of delays and advances in the pulse transmission time.

Subsequently, the signal begins its transmission process performing the reverse path to the one already explained. That is, it passes through a digital-to-analog converter (DAC) where the same errors related to the number of bits, DNL, offset, and gain of the converter transfer function are inserted. Subsequently, an up-sampling is performed to allow the up-conversion without the presence of the aliasing effect. To maintain phase coherence, the same initial LO is used for this last process. Finally, a low-pass filter removes any frequency components that are above the sampling rate of the signal, which is ready to be transmitted [13].

In the search for an initial simulator validation, a comparison between the simulator output signal and the theoretical predictions based on the literature was carried out. The general characteristics of the pulse were compared in several aspects. Specifically on the errors generated by random jitter, quantization, and DNL, using 1, 2, and 3, the theoretical values were calculated and compared with the measured errors in the simulator. Fig. 3 shows the results of a 10 bits ADC with 0.1 DNL error and random jitter of 60 ps rms. Irrelevant differences from the theoretical values can be seen because of the presence of thermal noise and random jitter behavior.

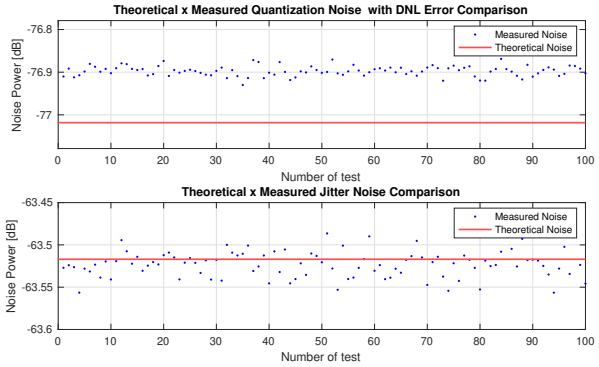

Fig. 3. Comparison of the errors generated in the DRFM simulator with those predicted by the theory.

III. Emulation Methodology

Despite having good results in comparing the output signal of the DRFM simulator and the one predicted in the literature, it is necessary to find a way to validate the model using real equipment. Therefore, electronic hardware instruments were used, each representing a specific part of the simulator. Once working in an integrated way, the combination of all these hardware has the same effects in terms of signal degradation as one would have in a real DRFM.

To set up the emulator, the one proposed by [6] was used since it meets the purpose of the experiment. Thus, the hardware that performs the function of signal reception, filtering, down-conversion, down-sampling, and digitization (including their respective errors) is the Digital Storage Oscilloscope (DSO X-92004) from Keysight. The hardware that performs the role of DAC, up-sampling, up-converter, filtering, and signal transmission, also with all errors and noise, is the Arbitrary Waveform Generator (AWG M-8190A) from Keysight. The simplified structure of the experiment is seen in Fig. 4.

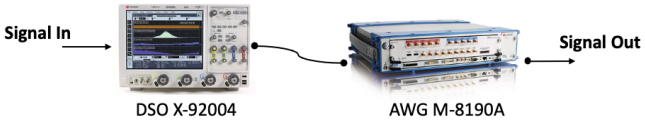

Fig. 4. Emulation structure used in the experiment.

For a correct comparison between the simulator and emulation signals, that model must be configured with the same parameters as the AWG and DSO. To this end, the Data sheets of each device were checked for their main characteristics. Briefly, the DSO operates up to 20 GHz and has an ADC that, despite having 8 bits, has a calibration table that provides digitized data with 16 bits. In addition, it has an approximate random jitter of 0.5 ps rms and an average DNL error of 0.05 LSB. The AWG used has a 14-bit DAC with a random jitter of 5 ps rms. Both systems are connected by two conventional SMA cables. One of them for the pulse transmission and the other to ensure that both devices operate synchronously.

Before the start of the emulations, the rms value of the thermal noise present in both devices was measured, and the same noise was inserted in the DRFM simulator. Then, two different waveforms were generated. The first one is a sinusoidal pulse with a frequency of 1 GHz. The second is a linear frequency modulated (LFM) pulse centered at 1 GHz. The general characteristics of these two signals are summarized in Table I.

TABLE I
PULSE CHARACTERISTICS

Parameter	Sinusoidal Pulse	LFM Pulse
Frequency (GHz)	1	1
Pulse Width (μs)	50	50
Bandwidth 3dB (kHz)	16.9	4757.2
Amplitude (V)	0.25	0.25
Sampling Rate (GHz)	4	4
LFM Rate (GHz/s)	–	100

Separately, the pulses were injected into both the DRFM simulator and the DSO+AWG emulation system. Subsequently, a comparative analysis of the characteristics of each pulse at the output of the systems was performed. In order to ensure the fidelity of the tests, 20 rounds of experiments were performed. The structure of the experiment is presented in Fig. 5.

Fig. 5. Setup used in emulation.

IV. Results

The first analysis of the output signals of both scenarios (simulated and emulated) is in the time domain. As seen

in Fig. 6, it is verified that the pulse width is practically the same for the two signals, with a difference of only 0.0056% for the sinusoidal one and 0.0044% for the LFM. However, there is a noticeable difference in the amplitude of the simulated and emulated signal in both cases. There are two explanations for this discrepancy. The first one is the existing attenuation in the cable used for the 1 GHz frequency. After performing its characterization, it was found that the attenuation is approximately 0.5 dB.

The second factor refers to the frequency response of the analog-to-digital converter of the DSO and the digital-to-analog converter of the AWG. Information taken from the Data Sheet of these devices shows that, for the operating frequency and sampling rate, there is an attenuation of approximately 1 dB in each hardware. Thus, the total attenuation of the system is approximately 2.5 dB, which justifies the difference in amplitude of the emulated and simulated signals.

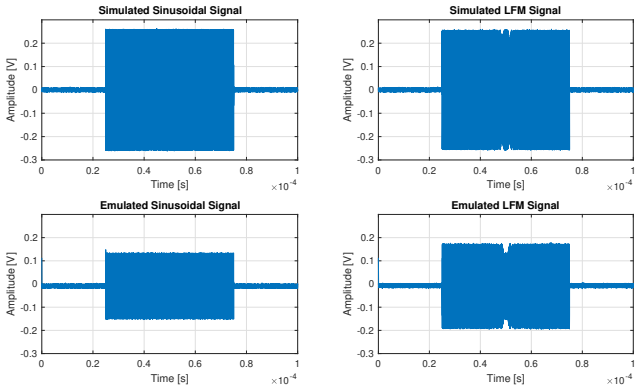

Fig. 6. Output signals in the time domain.

A second analysis of the pulse characteristics was performed in the frequency domain. For the sinusoidal pulse, as shown in Fig. 7, it is verified that the power of the emulated signal is 2.6932 dB lower than the power of the simulated signal. This discrepancy is within expectations, given the attenuations mentioned above. Discounting the system attenuation, the difference in amplitudes would be only 0.1932 dB or 0.7941%.

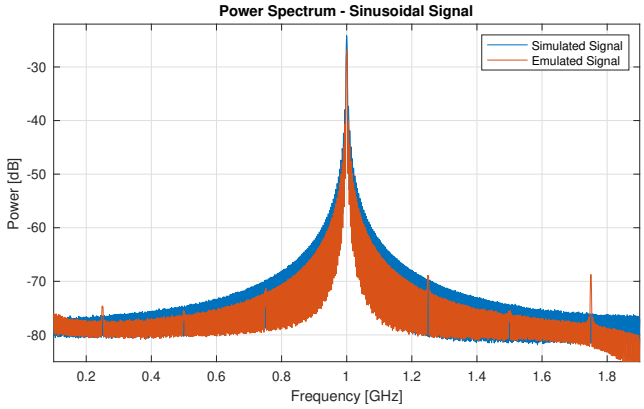

Fig. 7. Sinusoidal pulse in the frequency domain.

However, the presence of spurious signals at 250 MHz, 500 MHz, and their multiples with powers reaching values up to -68.72 dB is verified. The explanation for the appearance of these harmonics comes from the non-linear behavior of existing components in the AWG and DSO, such as amplifiers and etc. It should be noted that these errors were not modeled in the DRFM simulator, so they do not appear in the simulated pulse.

The same considerations can be made for the LFM pulse, as shown in Fig. 8. The power difference, in this case, is slightly higher, about 3.0425 dB, but still within the expected given the attenuations already mentioned. This difference drops to 0.5425 dB or 2.0547% when the necessary corrections are applied. Similarly to the previous case, the presence of spurious signals also occurs for the LFM pulse reaching values up to -68.43 dB.

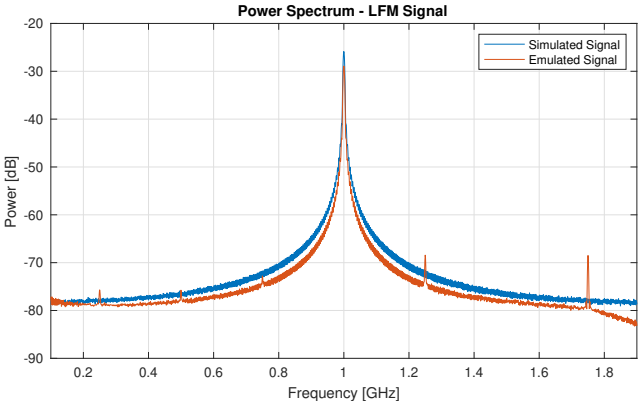

Fig. 8. LFM pulse in the frequency domain.

Another way to analyze the signals is by calculating the power spectral density. Fig. 9 shows this analysis for the sinusoidal pulse. In general aspects, a similar level of the noise floor is observed for both the simulated and the emulated pulse with a difference of 0.1852% between them. This factor is important because the noise floor level is directly related to the random jitter as well as the number of bits of the converters and their DNL. The fact that both are similar is an indication of the simulator's fidelity.

The enlarged part of the graph shows that the general characteristics of both pulses are maintained. The half-power bandwidth (frequency corresponding to a drop of 3 dB from the peak) of both pulses can also be measured. The values for the simulated and emulated signals are 16.974 kHz and 17.338 kHz, respectively.

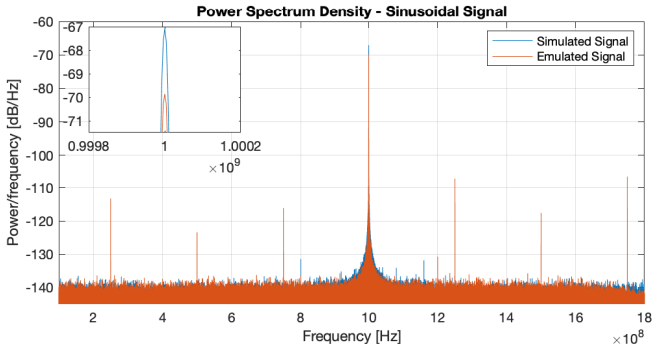

Fig. 9. Power spectral density of the sinusoidal pulse.

The same considerations regarding the equality of the noise level can also be made for the analysis of the spectral potential density of the LFM pulse shown in Fig. 10, finding

a difference of 0.1851%. Likewise, the general characteristics of the LFM pulse are observed to be maintained, as visualized in the enlarged image, except for a spike present exactly at 1 GHz in the emulated signal. As for the half-power bandwidth, the values for the simulated and emulated pulses are 4.756 MHz and 4.768 MHz, respectively.

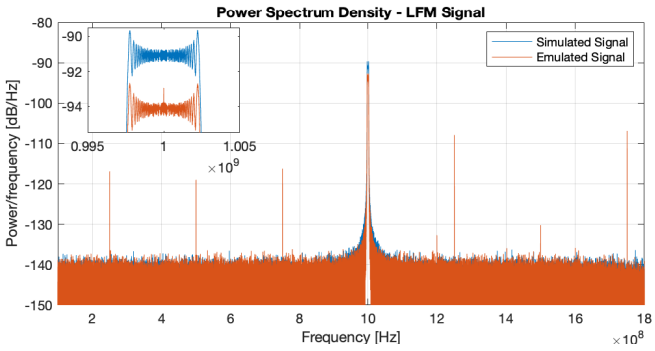

Fig. 10. Power spectral density of the LFM pulse.

Finally, another important characteristic of the pulse to be analyzed can be observed in the spectrogram of Fig. 11, where it can be observed that both the simulated and emulated pulses of the sinusoidal signal maintained their frequency and power characteristics over time. Both present similar intensities (except for the already mentioned attenuations) in the same time interval. As for the LFM pulse, the same can be verified. It is noticed that both pulses maintain the same rate of frequency change. More precisely, the difference between the LFM rate of both signals is only 0.31%.

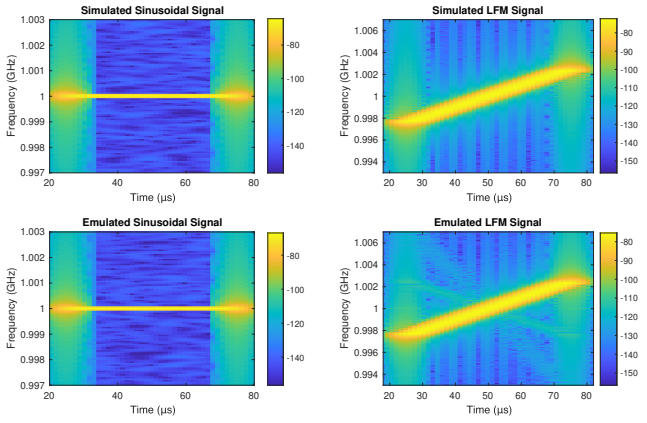

Fig. 11. Spectogram of simulated and emulated pulses.

To facilitate comparison, Table II presents a summary of the characteristics of each of the setups performed. It can be seen that the difference in the pulse parameters found was minimal, which means that both models degrade a signal equivalently. It can therefore be said that, given the appropriate limitations of the model, the DRFM simulator is similar to its real equivalent system.

V. Conclusion

Building a DRFM simulator to analyze its variables and parameters brings great benefits and advantages to studying its effectiveness in generating signal reliability. However, it is necessary to find a way to validate the simulator.

TABLE II
PULSES COMPARATIONS

SINUSOIDAL SIGNAL

Parameter	Simulation	Emulation	Δ%
Peak Power (dB)	-24.135	-24.328*	0.7941
Sidelobe Level (dB)	-37.3117	-37.5024*	0.5111
Pulse width (μs)	50.003	50.000	0.0056
Bandwidth 3dB (kHz)	16.974	17.338	2.1019
Frequency (GHz)	1	1	0.0000
Noise Floor (dB)	-145.789	-145.519	0.1852

LFM SIGNAL

Parameter	Simulation	Emulation	Δ%
Peak Power (dB)	-25.861	-26.403*	2.0547
Sidelobe Level (dB)	-40.9412	-41.4758*	1.3058
Pulse width (μs)	50.006	50.003	0.0044
Bandwidth 3dB (MHz)	4.756	4.768	0.2376
Frequency (GHz)	1	1	0.0000
Noise Floor (dB)	-145.806	-145.537	0.1851
LFM Rate (GHz/s)	97.689	97.994	0.3105

* Disregarding attenuation

The considered validation process used in this paper was an emulation procedure using DSO and AWG hardware to reproduce the effects of a DRFM and compare them with the investigated simulator. The results were satisfactory for all analyzed pulse parameters. Once some specific characteristics were compensated, the variations between the simulated and emulated pulses were minimal. This conclusion allows us to infer that both the DRFM simulator and the emulation system operate very similarly, validating the model.

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